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August 4
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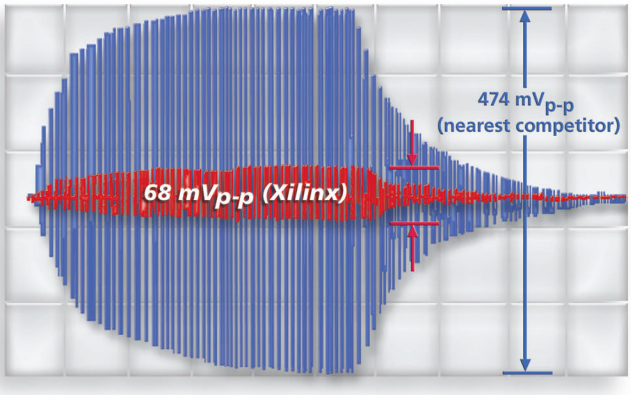
THE 32ND ANNUAL MICROPROCESSOR DIRECTORY

CHARTING YOUR COURSE

Page 57

"High Signal Integrity Demands A Low-Noise Chip".



Design Example: 1.5 volt LVCMOS 4mA, I/O, 100 aggressors shown.

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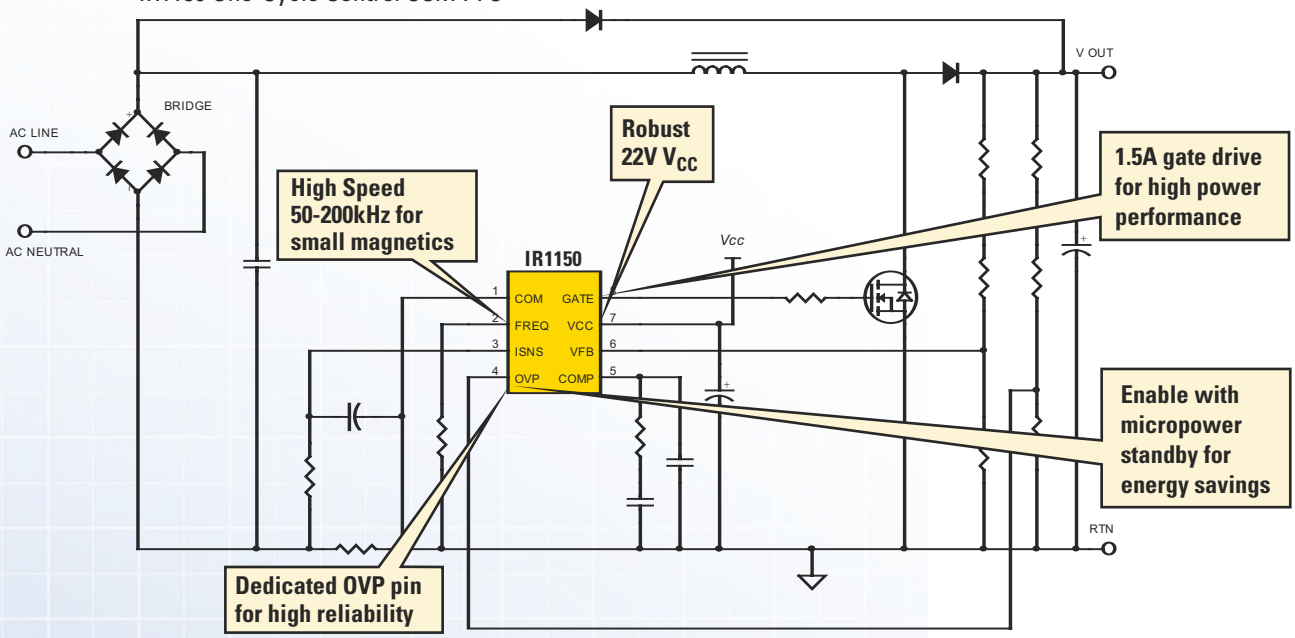

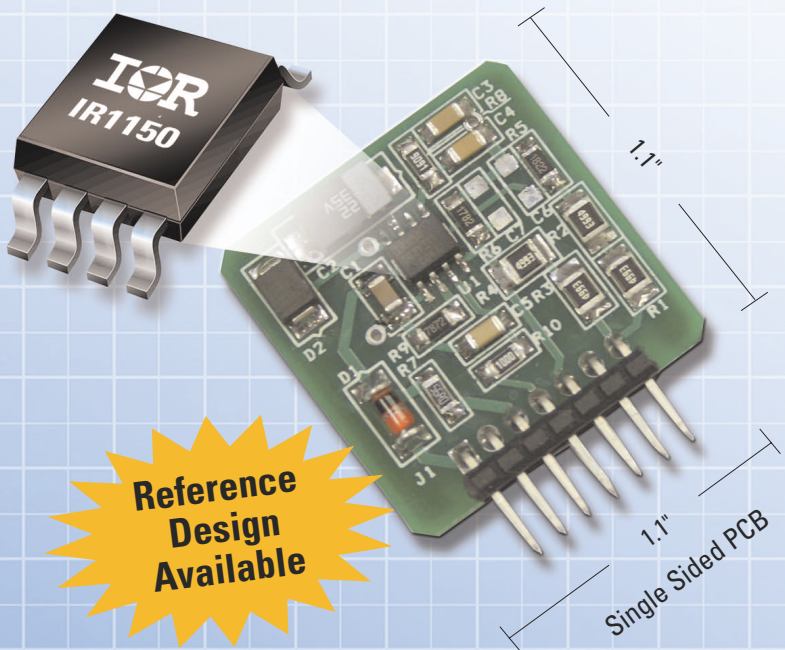

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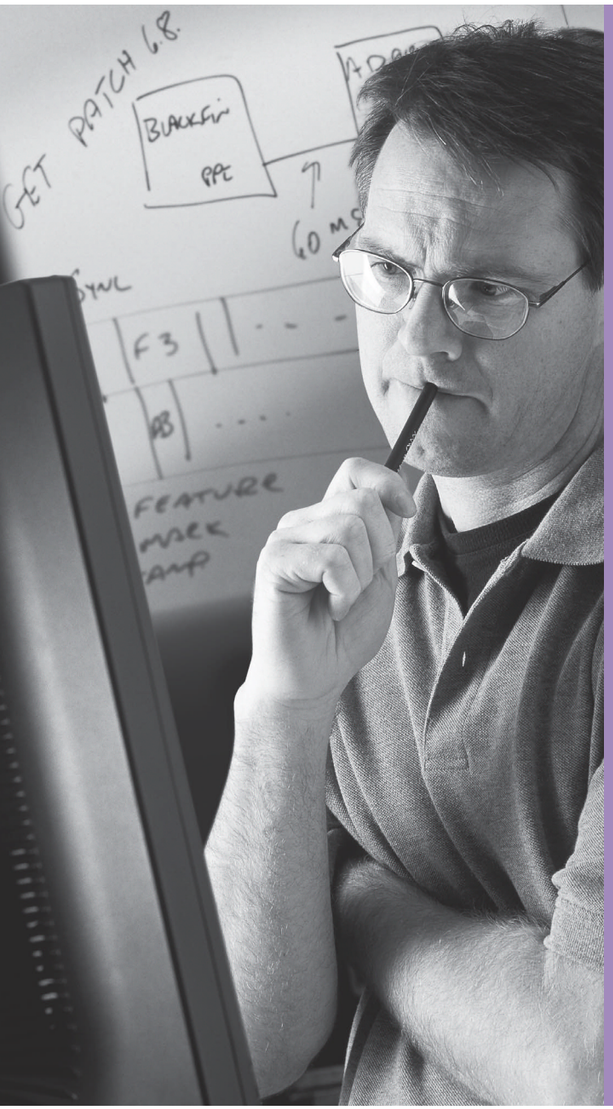

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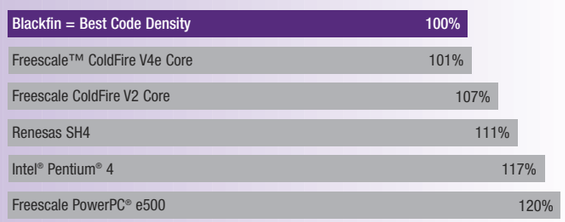
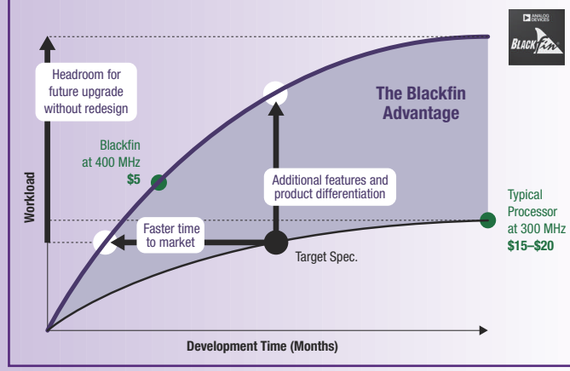


Relative code size comparisons for third-party benchmarks using Green Hills Software's MULTI Compilers.

Blackfin Programming Benefits vs. Typical Embedded Processor



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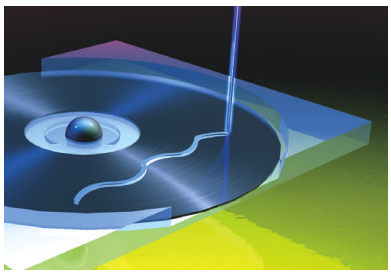
The 32nd Annual Microprocessor Directory: charting your course

by Robert Cravotta, Technical Editor



Beating the blue-laser blues

by Brian Dipert, Senior Technical Editor

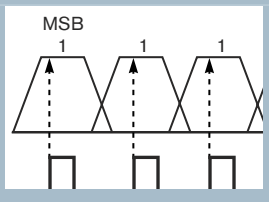
WiFi and Bluetooth fight for bandwidth

by Richard A Quinnell, Contributing Editor

Choosing and using microprocessor memory interfaces

by Victor Echevarria, Rambus

DESIGNIDEAS



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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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More Microprocessor Directory

Head to **www.edn.com/050804cs** for online-exclusive additions to this issue's Microprocessor Directory (pg 57), including a comprehensive table of technical details on available devices and cores.

In addition, check out these archived articles ...

2004 Microprocessor Directory: Last year's edition of Technical Editor Robert Cravotta's compendium of microprocessor and microcontroller information.
➔www.edn.com/article/CA438294

2005 DSP Directory: The most recent edition of our annual guide to DSP chips and cores.
➔www.edn.com/article/CA526330

From the vault

Articles related to "WiFi and Bluetooth fight for bandwidth" (pg 73):

Regulating the playpen: From *EDN Europe*
➔www.edn.com/article/CA431198

Bluetooth interoperability: It's all in the details
➔www.edn.com/article/CA293236

Our new department, "Prying Eyes," in which we get inside a new gadget or technology, makes its third appearance in this issue ("Cheap shot," pg 32). In case you missed the earlier installments, here they are:

Contactless traveling: Electronic passports
➔www.edn.com/article/CA621643

In the game? Nintendo's DS handheld
➔www.edn.com/article/CA605509

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Tool promises faster Matlab simulation
Catalytic has released a tool that it claims can speed up Matlab simulation 10 to 200×.
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IP vendors unite to ease USB headaches
TransDimension and ChipIdea have announced a partnership that combines the former's USB controller and software with the latter's USB PHY.
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BY JOHN DODGE, EDITOR IN CHIEF

Who's next after Unocal, Maytag?

Successful or not, China's state-owned oil company's bid to acquire Unocal and Haier Group's same plan for Maytag will reverberate throughout the American industry. Such intentions have implications far beyond each individual transaction, should any come to pass.

At a philosophical level, the US rejection of Chinese takeovers would be extremely hypocritical. The admonition "be careful what you wish for" couldn't be more appropriate with respect to China, given how the United States tried to open up the world's most populous nation for decades. China is very open now—open to an unprecedented buying spree.

"If the market is such that Chinese companies are bidding for American companies, why not? I don't see how you can stop it unless there are national-security concerns. It's not any different from Japan's buying spree in the '70s and '80s," says Jim Williams, staff scientist at Linear Technology.

Hypothesize for a moment that China Integrated Circuit Design Corp Ltd comes after American high-tech-icon Texas Instruments (**Link 1**). Given China's $700 billion in cash reserves, the scenario is not that far-fetched, even though TI's market cap hovers around $35 billion. (For the sake of comparison, Intel's market cap is $160 billion, and Microsoft's is $270 billion.)

National-security concerns could easily come into play, because electronics form the core of most weapons systems. China's access to TI's myriad IP (intellectual property), enormous brainpower, and thousands of patents could come back to haunt the United States if hostilities ever ensue.

But think about it. Paying for IP—not to mention protecting it—would be a new game for the Chinese. Legitimate ownership of highly valuable IP in China is probably something the United States wants. As one news commentator recently noted, the value of pirated software and entertainment in China could wipe out the US trade imbalance—$56.7 billion through the first four months of this year (**Link 2**).

Paying for IP—not to mention protecting it—would be a new game for the Chinese.

"It would also be interesting to see people pile out of a company they've bought. Chinese companies aren't used to a mobile work force," adds Williams. Indeed, core assets of any design company are its collective brilliance and knowledge.

The acquisition of TI or any other American electronics company could be just around the corner. It was once unimaginable that Lenovo could buy IBM's struggling PC business, but Lenovo did, although IBM's PC business was very much for sale.

Prevailing US and Chinese laws should allow the Unocal and Maytag episodes to reach their natural conclusions (**Link 3**). Here's hoping that these companies don't become political footballs, with each side trying to extract concessions that don't relate to the acquisitions; plenty of unresolved issues already exist between the two superpowers. China will eventually award third-generation licenses. The United States wants help with North Korea, and it also wants China to float the yuan on the open currency market. China wants Taiwan to rejoin the mainland. Human rights are always on the table.

Much has changed since I visited Beijing with my family in April 1999, just before a B2 bomber released a smart bomb on the Chinese embassy in Belgrade, Serbia (**Link 4**). Tiananmen Square was closed for a supposed makeover to commemorate the 50th anniversary of the communist takeover. We suspected that its closure was to avoid calling attention to the 10th anniversary of the Tiananmen uprising as well (**Link 5**).

That's all history. China now has only unbridled enthusiasm for taking its rightful position as an economic superpower. EDN

MORE AT EDN.COM

Should the United States let Unocal and Maytag go? Post your comments on the Feedback Loop at www.edn.com/050804ed1.

WEB LINKS

1 www.cec.com.cn/cecchannel/english/cecchannel/product/product_011.html.
2 www.census.gov/foreign-trade/balance/c5700.html#2005.
3 http://news.xinhuanet.com/english/2005-06/29/content_3150261.htm.
4 http://kosovo99.tripod.com/chinese.htm.
5 http://en.wikipedia.org/wiki/Tiananmen_Square_protests_of_1989.

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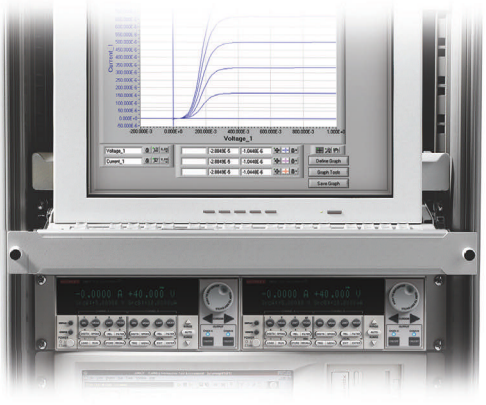

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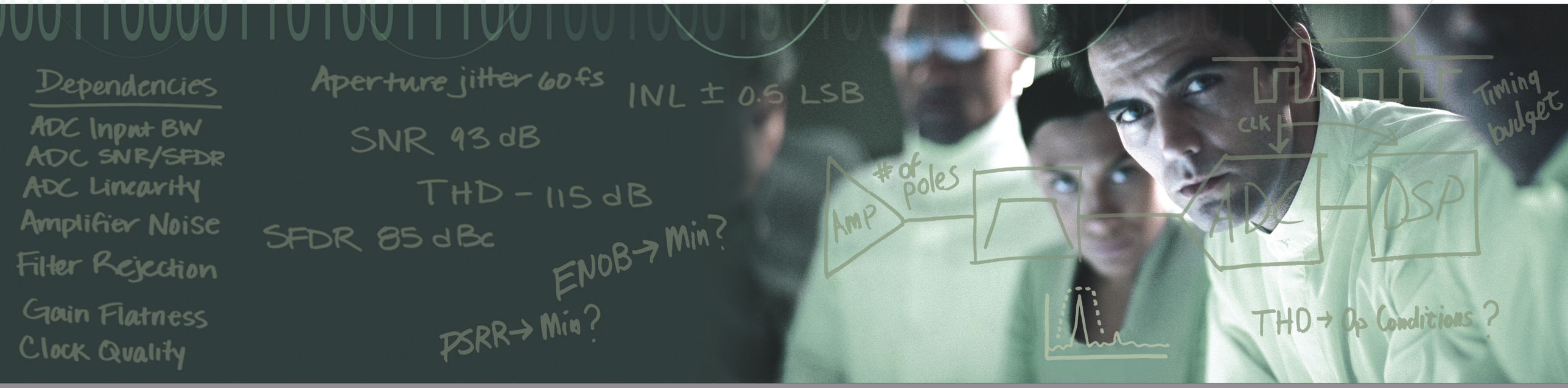

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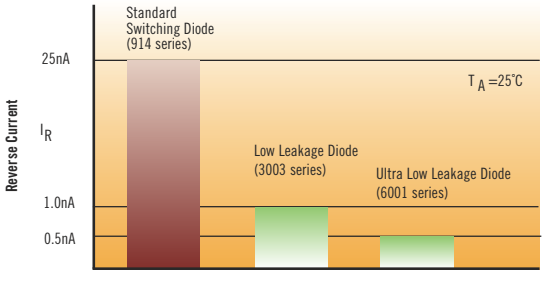

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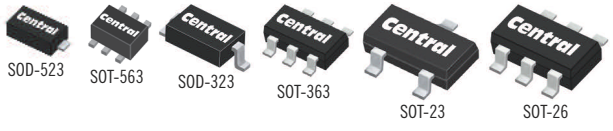

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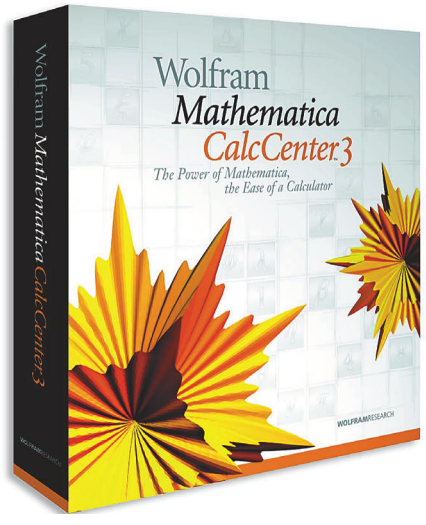
Easy-to-use math software promises Mathematica's speed and accuracy



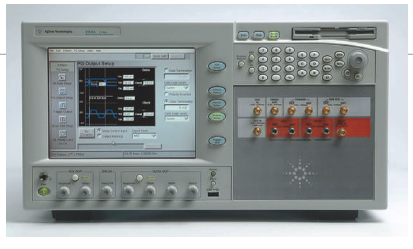
According to the vendor, Mathematica CalcCenter 3 combines the speed and accuracy of its progenitor, Mathematica, with extreme user friendliness and complete file compatibility with the established package.

Wolfram Research says that its new Mathematica CalcCenter 3 delivers the speed and accuracy of the company's flagship Mathematica package in a version that new users can get up and running in as little as 10 minutes. The target audience for the new package includes users who believe that their computational requirements have outgrown the capabilities of Excel, Mathcad, or Maple. CalcCenter 3 not only brings new speed and accuracy to high-powered math software, says a company spokesperson, but also is fully compatible with Mathematica itself. You can move notebook files back and forth between Mathematica and CalcCenter 3 as often as you wish. The underlying algorithms and technology are identical, and the speed with which CalcCenter 3 obtains results is just as great as that of its more powerful sibling.

Wolfram also says that, by leveraging the development of CalcCenter 3 on the established Mathematica, it reduced development costs and thereby more attractively priced the easy-to-use package than it could have had it built the new package from the ground up. Mathematica CalcCenter 3 carries a list price of $595 in the United States and Canada. The academic list price is $195, and a student version costs $99.95.**—by Dan Strassberg**

▷**Wolfram Research Inc,** www.wolfram.com.

Serial-pulse-data generator produces 7-GHz patterns



The 81141A provides serial pulse trains at rates to 7 GHz for physical-layer testing of ultrahigh-speed serial buses.

Agilent Technologies has announced a high-speed, serial-pulse-data generator with stimulus capability to 7 GHz. According to the company, the 81141A is the first pulse generator to achieve such speeds. By providing precision low-jitter signals and offering full control of data streams for stress tests, the $88,000 instrument enables computer- and semiconductor-test engineers to accurately characterize components for the next-generation, high-speed serial buses. The unit's 1-GHz linear-delay modulation enables fast and precise jitter-tolerance and jitter-transfer measurements.

"Combining multiple data formats, such as RZ [return to zero], R1 [return to one], and NRZ [non-return to zero], with sequencing, trigger capability, and fast frequency change, is unique in the market and is critical for the next-generation high-speed-technology wave," says Siegfried Gross, vice president and general manager of Agilent's Digital Verification Solutions Division. "High-speed design starts with the physical layer and its signal integrity."**—by Dan Strassberg**

▷**Agilent Technologies,** www.agilent.com/find/7g_pulse.

Bluetooth chip targets stereo headsets

Broadcom has rolled out its first Bluetooth chip for wireless-stereo headsets. The single-chip BCM2037 includes Bluetooth EDR (enhanced-data-rate) functions for enhanced audio quality and extended battery life. Broadcom officials state that this chip is the first Bluetooth chip it has released since the March 2005 acquisition of wireless-audio-technology vendor Zeevo Inc.

Scott Bibaud, Broadcom's Bluetooth marketing manager, says the BCM2037 leverages Broadcom technology and Zeevo's 4301 Bluetooth chip set. He notes that, by being EDR-functional, the chip now complies with Bluetooth 2.0 plus EDR, tripling its data rate to 3 Mbps from 1 Mbps, previously the highest data rate on a Bluetooth 1.1 platform. The BCM2037 also offers lower power consumption through Bluetooth-based products with its stereo-streaming capability. This process includes transmitting data from host-side, or transmitter, products—such as PDAs, PCs, or cell phones—to stereo headsets on the receiver side. The lower power consumption gives users longer headset-battery life by allowing them to stream data for as long as 10 hours at 3 Mbps, rather than six at 1 Mbps.

Longer battery life and power-consumption factors are attractive to engineers considering using the BCM2037, and a higher data rate prevents users from hearing sound gaps and data errors. The headset works effectively in longer ranges, because the data moves faster and is more robust. According to Joyce Putscher, director of converging markets and technologies at In-Stat/MDR, the ARM7 processor, which powers the chip, helps expedite the data flow, and many engineers have used it. More important, Putscher notes, is the increased battery life and low power consumption. "When you can design something that can use a smaller battery, you can potentially reduce design costs, as well as increase battery life," she says. Another advantage is that engineers and designers might be able to design around either a smaller and cheaper battery or provide product differentiation with a longer battery life.

Broadcom's BCM2037 is currently available for sampling to early-access partners and will go into full production during the third quarter. The sample price is less than $10. This year, Broadcom also released the BCM2045, an EDR chip for cell phones, notebook computers, and other devices. "We are trying to improve the overall user experience by aggressively bringing EDR to the market, as well as improving audio-video-streaming capability," says Bibaud.—**by Jeff Berman**

▷**Broadcom,** www.broadcom.com.

FEEDBACK LOOP

"The problem that engineering work has is really an American societal problem. Jobs that receive the most compensation are generally jobs that deal with money—management, sales, CPAs, bond trader, etc—rather than jobs that create money (engineering, skilled labor, etc). If you want to see the end result of this, study the Roman Empire."

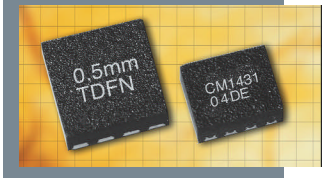
Joel Fields, in *EDN*'s Feedback Loop on www.edn.com/article/CA608159. Add your comments.

DILBERT *By Scott Adams*

08.04.05

Tiny filter repels EMI/ESD away from wireless functions

As wireless phones get smaller and pack in more auxiliary functions, such as cameras, the potential for EMI problems increases, whereas the space available to squelch these problems shrinks. To address these issues, the Centurion CM1430 and CM1431 filter arrays from California Micro Devices combine EMI



Small—but with big EMI attenuation and ESD protection—the CM1430 and CM1431 filters have a 0.4-mm pitch and a 0.4-mm profile.

filtering with ESD protection in a low-profile, 0.4-mm-high package. These four-, six-, and eight-channel devices implement capacitor-resistor-capacitor pi-filter topologies with cutoff frequencies of 200 and 120 MHz. The CM1430 and CM1431 offer 1-GHz attenuation of 25 and 35 dB, respectively.

ESD protection reaches ±15-kV contact discharge, as IEC61000-4-2 Level 4 specifications dictate. Lead pitch is 0.4 mm, compared with 0.5 mm for previous packages. The 0.1-mm difference results in a board-footprint reduction as great as 40%. Devices cost 42 to 59 cents (1000).

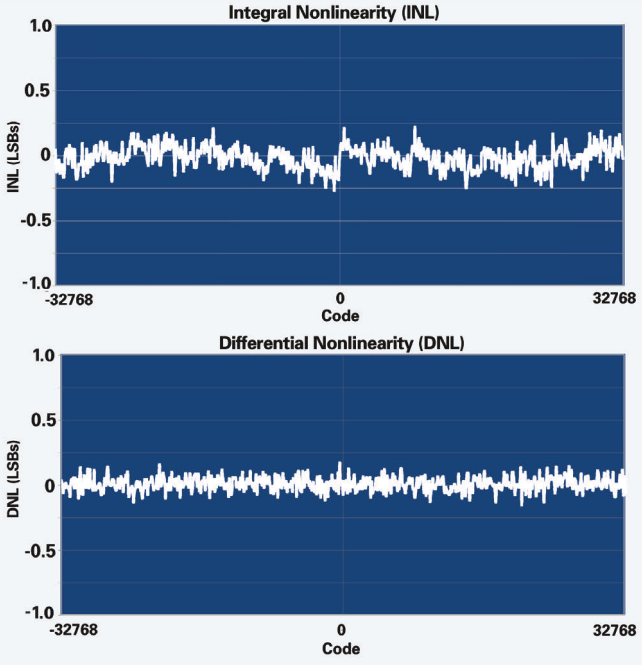
—by Bill Schweber

▷California Micro Devices Corp, www.calmicro.com.

DATA CONVERTERS

Most Linear 16-Bit SAR ADC

<0.75 LSB INL and <0.5 LSB DNL Over Temperature



The **ADS8372** high-performance ADC from Texas Instruments features 16-bit no missing code performance, 600kSPS data rate, less than 0.75 LSB INL and less than 0.5 LSB DNL over the entire industrial temperature range (–40°C to +85°C). Complete with internal reference and reference buffer, the ADS8372 provides breakthrough signal linearity without requiring active external components, enabling new levels of system performance in advanced, real-time applications.

▶ Applications

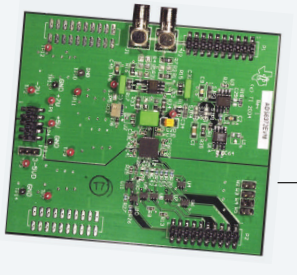
- Automated test equipment
- Medical imaging
- Optical networking
- High-speed control loops
- High-resolution data acquisition systems

▶ Features

- 16-bit, 600kSPS data rate
- INL: ±0.75 LSB (max)
- DNL: ±0.5 LSB (max)
- Offset drift: ±0.2ppm/°C
- SNR: 94dB
- Internal reference
- Internal reference buffer
- Compatible with TI's TMS320™ DSPs
- Easy prototyping with TI's modular evaluation system
- 28-lead 6x6mm QFN package
- $13.00/1K price

New High-Performance 16-Bit ADCs

Device	Input Range (V)	Speed (kSPS)	INL (LSB)	DNL (LSB)	SNR (dB)	Interface
ADS8372	±4.096 at 2.048	600	±0.75	±0.5	94	Serial
ADS8370	4.096	600	±1.25	±0.75	90	Serial
ADS8509	±10, ±5, 10	250	±2	±1	88	Serial
ADS8410	4.096	2000	±2.5	–1, +1.5	87	Serial LVDS
ADS8413	±4.096 at 2.048	2000	±2.5	–1, +1.5	92	Serial LVDS
ADS8411	4.096	2000	±2.5	–1, +2	86	Parallel
ADS8412	±4.096 at 2.048	2000	±2.5	–1, +2	90	Parallel



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Texas Instruments

Software targets communications design

The Mathworks recently rolled out Communications Blockset 3, an upgraded version of a software program that offers engineers added functions for designing and simulating the physical layer of communications systems and components for wireless and wireline systems using model-based design. The new version, which includes channel visualization and bit-error-rate-analysis functions, lets users exchange and share executable specifications throughout the modeling and simulation process. These functions allow designers to view various channel-mode-domain behaviors, such as time, frequency, and phasor, to design communications receivers and to compare simulation results with benchmarks in a GUI setting.

Colin Warwick, communications-products manager at The Mathworks, says that Communications Blockset 3 helps improve communications-product design. "Communications products are becoming more computationally intensive than they were in the old days when engineers and designers relied on paper-based models, which were time-consuming and made it hard to 'tease out' design errors with Spice error codes and netlists," says Warwick.

Model-based design provides a working model of a communications-product design in a test environment to specify a product's behavior before a designer configures the part in hardware or software. "[Engineers and designers] want to focus on building products, not channel models," says Warwick. "This platform prebuilds a wireless channel, letting people focusing on building equalizers and similar products overcome channel impairments." Designing wireless channels is more challenging than building wire-line ones, due to communications products and devices that must adapt to changing landscapes, conditions, and speeds.

The channel-visualization features are particularly helpful for receiver designers, because they let them fix damage that changing conditions cause, says Mike McLernon, senior team leader for communications development at The Mathworks. "When collecting data, channel visualization lets users focus on specific channel characteristics, rather than signal characteristics, such as spreading, 802.11a, or MOFDM [multilevel-orthogonal frequency-division multiplexing]. This tool can slice into a time or a phasor domain and look at channels at different angles to build receivers that combat the effects of signal characteristics," he says.

The bit-error-rate function lets users working at the physical layer of a design check testbench results against their own work to see where their results should be and how they match up. The tool automates comparisons and simulation results, so that designers can view them in a GUI environment to compare simulations with theory and integrate environments to combine simulation and analysis. This process helps gives users a clear indication of when a design is complete by plotting parameters, such as SNR versus bit-error rate.

Communications Blockset 3 also includes a synchronization library, which lets users build receiver models without writing C code and model adaptive and nonadaptive algorithms. The Mathworks' Communications Blockset 3 is now available and costs $1000. The platform runs as part of the company's flagship applications, Matlab and Simulink.

—by Jeff Berman

▷**The Mathworks**, www.mathworks.com.

FEEDBACK LOOP

"We in America are about to discover the harsh reality that our technology is in the heads of the engineers. You lose those heads; you lose the technology. The Chinese realize this. We are in for some very hard times."

Anthony Mendoza, in *EDN*'s Feedback Loop on www.edn.com/article/CA526328. Add your comments.

According to the supplier, ATEasy's plug-in fault library and fault editor enable test engineers to develop applications that simplify diagnosis and repair of faults in units under test.

Test executive/development package adds fault library and editor

08.04.05

Geotest-Marvin Test Systems has announced the addition of a fault-library plug-in module and a fault editor to its $3995 ATEasy 5.0, vendor-independent, open-architecture test executive and rapid-test-application-development software package. According to the company, ATEasy combines the ease of use of Visual Basic with the flexibility of C++. Event-driven programming style maximizes code efficiency, and compiled code speeds program execution. User-defined plain-language commands ease code maintenance, and built-in configuration-management tools simplify project management. Application wizards quickly guide new users through development projects.

The plug-in fault-library software tool facilitates troubleshooting of electronic circuits. The library allows test engineers to create fault dictionaries that provide users of ATEasy applications with simplified diagnostic capabilities. The fault editor allows program developers to define fault conditions that ATEasy will analyze at runtime.

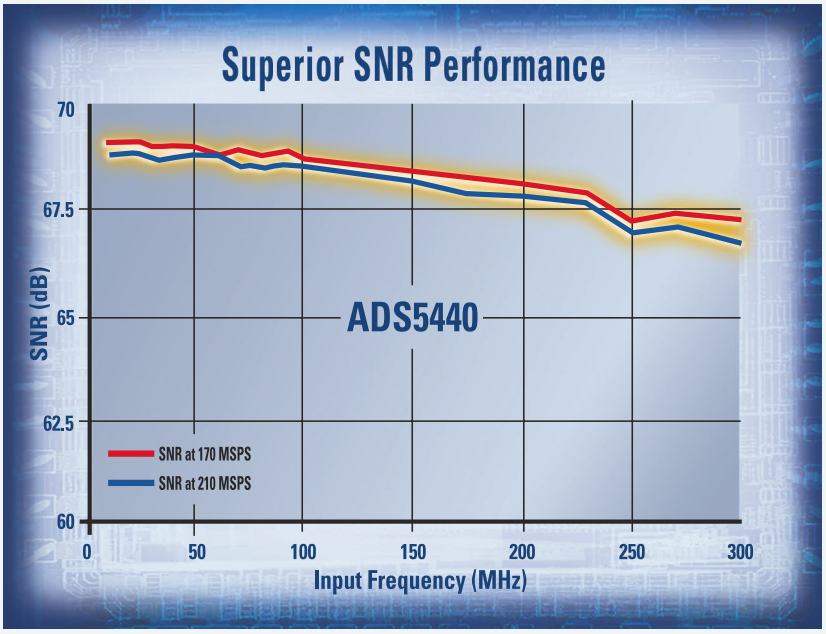
—by Dan Strassberg

▶Geotest-Marvin Test Systems Inc, www.geotestinc.com.

DATA CONVERTERS

13-Bit, 210 MSPS ADC

Superior SNR Performance. Now!



The **ADS5440** high-speed analog-to-digital converter from Texas Instruments features superior dynamic performance at high input frequencies. Providing break-through SNR performance, the ADS5440 enables improved receiver performance in multi-channel base stations and software defined radio (SDR) applications, and improved sensitivity for test and measurement equipment.

Device	Resolution (Bits)	Speed (MSPS)	SNR (dBc)	SFDR (dBc)
ADS5440	13	210	68 at 170 MHz IF	77 at 170 MHz IF
ADS5500	14	125	69.5 at 100 MHz IF	82 at 100 MHz IF
ADS5424	14	105	74 at 50 MHz IF	93 at 50 MHz IF
ADS5541	14	105	71 at 100 MHz IF	86 at 100 MHz IF
ADS5423	14	80	74 at 50 MHz IF	94 at 50 MHz IF
ADS5520	12	125	68.7 at 100 MHz IF	82 at 100 MHz IF
ADS5521	12	105	69 at 100 MHz IF	86 at 100 MHz IF

▸ Applications

- Software defined radio
- Test and measurement/ instrumentation
- Base stations:
  - Multi-channel receivers
  - Transmit digital pre-distortion (DPD)
- Communication Instrumentation

▸ Features

- SNR = 68 dBc at 170 MHz F_{IN} and 210 MSPS
- SFDR = 77 dBc at 170 MHz F_{IN} and 210 MSPS
- SNR = 68 dBc at 230 MHz F_{IN} and 170 MSPS F_S
- SFDR = 80 dBc at 230 MHz F_{IN} and 170 MSPS F_S
- Supports the industrial temperature range of –40° C to +85° C
- 80-pin TQFP PowerPAD™ package
- Fully buffered input simplifies input circuit design
- Lead (Pb)-free/green
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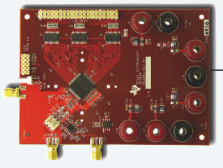

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Q&A
Bob Lucky
Hard work makes its own luck.

Robert "Bob" Lucky, PhD, is the former head of the legendary Bell Labs. Bell was the home of much of the vital research that our industry now employs, including the transistor. It also was the birthplace of some pure research having no apparent application, such as discovering that the omnipresent background noise of the universe is due to remnants of the big-bang theory. While at Bell, Lucky also played a key role in the development of adaptive equalizers' filtering strategy, a key component in all high-speed modems. He's also the co-author of the seminal textbook *Principles of Data Communications* and a long-running columnist in *IEEE Spectrum*.

What led you to become an engineer?

A When I was in high school, I didn't have a clue what engineers did. I was good in math and physics, and I liked to build radios and electronic equipment, so people said I should be an engineer. I marvel at how clueless I was. Now, after a long career as an engineer, I'm still not sure what they do.

I'll never forget my first week at college. I had to take mechanical drawing, and the instructor told us that all engineers had to start their jobs on the drawing board. That actually wasn't true even then, but I believed it—especially because I wasn't much good at mechanical drawing. During a test, I drew something badly, and, in exasperation, I threw my compass down on the drawing. It bounced off the drawing and flew out the open window next to me. I don't remember how I did on that test, but it couldn't have been good.

How did you get into writing your *IEEE Spectrum* column and other less-technical items?

A People sometimes ask me how they can get their own column, usually hinting that they could do better than I do. Sometimes, I tell them that you just have to be "lucky." In the early years of my column, I used to worry that someone would take it away from me. People would send me sample columns that they had written and copy the *Spectrum* editor. That hasn't happened now for a long time, and, after 23 years of writing the column, I don't really worry about things like that any more.

I owe the column to the *Spectrum* editor of 1981, who was Don Christensen. He had asked me to do a book review of Tracy Kidder's *The Soul of a New Machine*—still a great book, by the way—for the institute's newsletter. They liked my review and asked me to write a movie review of *Tron*.

Then, I wrote a review of Michael Crichton's *Congo* for *Spectrum*. I was quite abashed when Crichton himself sent a rebuttal to my review to *Spectrum*. I had said that his technology was faulty, and his rejoinder was that his book was fiction, and he could make up stuff. I agreed with this statement but said that the fact that he had included lots of references from IEEE journals gave the reader the idea that the technology was correct. In private communication, we both agreed that the other had a point. Moreover, I have to say that his subsequent novels all are based on great technical ideas.

After these reviews, Christensen suggested that I try a column and see how it went. The rest is history. It is truly a great privilege to have a column, and I often take a moment to appreciate the luck and the honor.

In the beginning, I had to submit my columns for clearance through the Bell Labs review process. I was embarrassed to do this, and, apparently, so were the reviewers. Then the public-relations department told me that maybe this clearance wasn't necessary—that I was on my own for these columns. Now, wherever I go, someone will come up to me and say that they like my columns. I never tire of hearing this, and, whatever work I do on them is worthwhile. People often tell me that I write well "for an engineer." I'm never sure whether this is a compliment.

Did you think your work at Bell Labs would have such a broad impact on digital communications?

A Actually, I've never thought that my work did have that kind of impact. I was fortunate to be in the right place at the right time, 1961, when modems were first being developed. I'm sure that, if I hadn't invented the adaptive equalizer, someone else would have done it a month later. Much of technology is like that. There are, of course, exceptions, and the great work of [the late] Claude Shannon, [the "father of information theory"], is the biggest exception to that general rule.

Any comments on the state of engineering and science education?

A People say it's bad, particularly math education in the secondary schools, but I haven't been involved in that issue. I have been concerned, however, with what an engineer should learn in college. I'm not sure I have any answers, but I do believe that, in college, you need to learn how to learn, and I'm not sure that this is a real focus. Everything I studied has been obsolete for decades. All that remains is a general engineering culture, some mathematical principles, and an ability to learn new things as time goes along.

—by Bill Schweber

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Go to www.edn.com/050804p1 for more from Bob Lucky in an expanded version of this interview.

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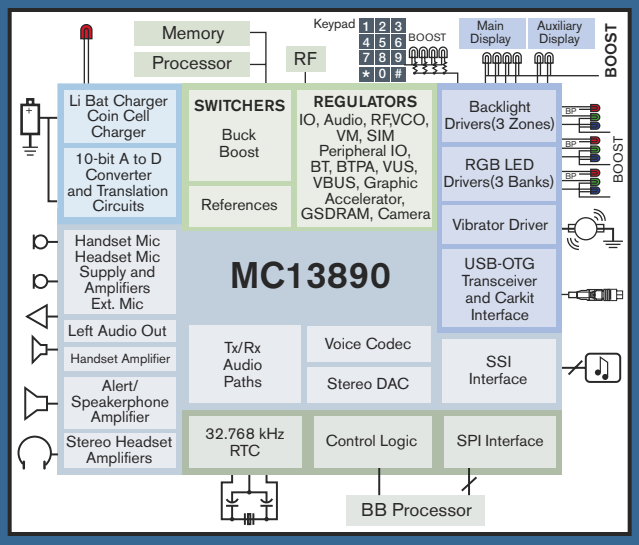

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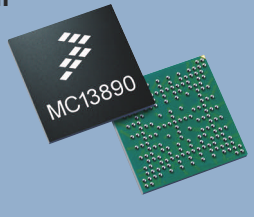

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GLOBAL DESIGNER

Chinese chip vendors push TD-SCDMA terminals

The TD-SCDMA Industry Alliance is this summer sponsoring field tests for TD-SCDMA (time-division synchronous-code-division multiple-access) networks in Beijing and Shanghai. If things go smoothly, separate trial TD-SCDMA-network subscriptions will be available within two to three months after completion of this summer's field tests. Yang Hua, secretary general of the TD-SCDMA Industry Alliance, says that the field tests are focusing on TD-SCDMA-network-infrastructure performance and reliability, interoperability between infrastructures and terminals, and performance of terminals. He adds that the results of these field tests will play a large role in determining whether TD-SCDMA commercialization can become a reality.

However, domestic vendors say that the maturity of TD-SCDMA terminals is the toughest issue for TD-SCDMA's commercialization. "The maturity of TD-SCDMA terminals will not come until mid-2006," says Luo Zhongsheng, assistant general manager of the handset unit of communications-product vendor ZTE (www.zte.com.cn). Chinese terminal-chip vendors, such as T3G (www.t3gt.com), Commit (www.commit.net.cn), and Spreadtrum (www.spreadtrum.com) are cooperating with system vendors to improve the interoperation between infrastructure and terminals.

In April, T3G introduced its chip sets for TD-SCDMA/GSM (global-system-for-mobile-communications) dual-mode terminals. The company has realized core functions, such as 384-kbps packet-data transfer, 64-kbps real-time circuit-data transfer, and cross-network wandering, through these offerings. T3G officials say that the company's dual-mode chip set interoperates with all TD-SCDMA networks from Datang Mobile (www.datangmobile.com), ZTE, and Putian (www.chinaputian.com). In June, T3G also unveiled an ASIC-based, high-speed PCMCIA data card, which allows notebook computers to successfully achieve 384-kbps packet-data transfer and conduct broadband multimedia services, such as Internet browsing, FTP downloading, and VOD (voice over data) through wireless packet networks.

Commit has launched its verified TD-SCDMA-terminal chip set, including baseband, RF, power management, a protocol stack, and a comprehensive development-and-test environment. The chip set supports 3G services, such as video phone, high-speed Internet browsing, and streaming media. Currently, some leading mobile-phone vendors, including LG, Lenovo, and Bird, have introduced their TD-SCDMA mobile phones based on Commit's semiconductor technology. Commit has passed IOT/COT (interoperability tests/continuity tests) on main network equipment from Datang Mobile, ZTE, Putian, and others.

Spreadtrum has also made smooth progress in the development of TD-SCDMA terminals. By teaming up with domestic mobile-phone vendors, such as Bird, it has developed a host of TD-SCDMA terminals. "The first TD-SCDMA subscribers are more likely to come from the voice market," says Yu Yushu, Commit's chief executive officer. "Data services are certainly important, yet the stable voice services will remain the biggest selling point at the outset." He says that WCDMA (wideband code-division multiple access) has a high place in the market, whereas GSM is on a relatively low level. He believes that TD-SCDMA will emerge in the middle but may be closer to GSM. **–by Harry Wang,** *EDN China*

▷**TD-SCDMA Alliance**, www.tdscdma-alliance.org.

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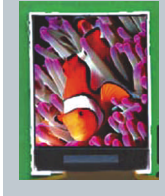
For more global news, visit www.edn.com/global.

LCD driver challenges TFT devices in mobile-phone applications

Targeting mobile phones that rely on color displays, Hong Kong-based Solomon Systech Ltd has launched the first device in a series of innovative CSTN (color supertwist-nematic) LCD drivers. The SSD1784 display controller can support 132×60-pixel-resolution CSTN LCDs. Using the SSD1784, you can achieve 65,000 color combinations in a simple application circuit.

The SSD1784 features a dual OTP (one-time-programmable) ROM, an eight-color power-saving mode, and divider-level accuracy-improvement circuitry. The SSD1784 has more features and uses smaller die than its SSD1783 predecessor and is software-compatible with previous devices from Solomon Systech, which means that designers can reduce development time using the controller.



The SSD1784 display controller can support 132×60-pixel resolution CSTN LCDs and achieve 65,000 color combinations in a simple application circuit requiring a microcontroller.

"CSTN LCDs are catching up with TFT [thin-film-transistor] LCDs in all aspects of display quality, including color depth, contrast, and viewing angle," says Eddy Luk, Solomon Systech's technical marketing engineer. According to Luk, CSTN LCDs also perform better than TFT LCDs in cost and cycle time in mass-production, and, for applications that require no ability to play video, CSTN is a good choice for cost, flexibility, and power consumption.

The SSD1784 offers partial-, sleep-, and eight-color standby modes. When you invoke the eight-color mode, the display controller's frame-rate control and PWM circuitry partially turn off. These circuit blocks generate gray-scale levels for RGB signals. Circuitry on the controller allows you to display red, green, blue, cyan, yellow, magenta, black, and white colors.

–by NS Manjunath, *EDN Asia*

▶**Solomon Systech Ltd**, www.solomon-systech.com.

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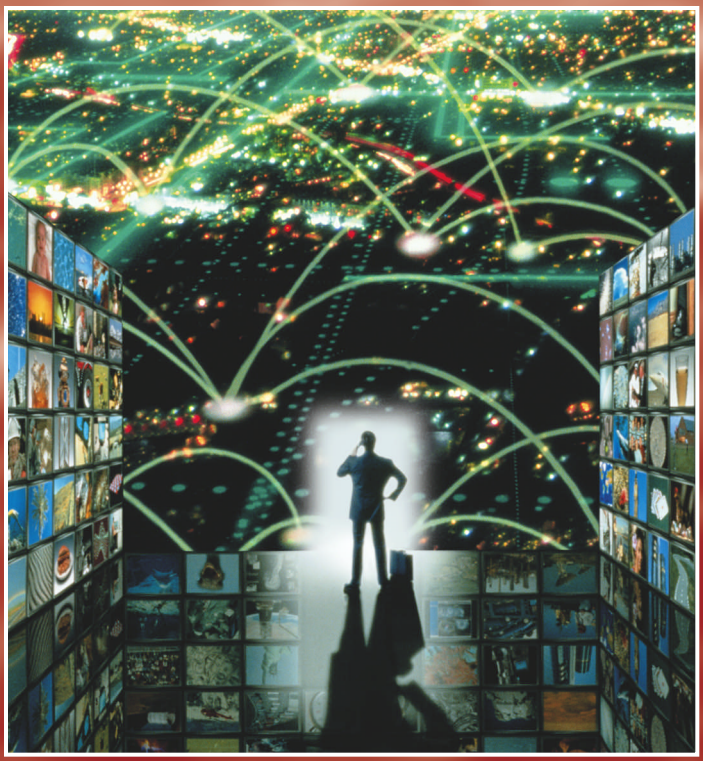

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Media Access Gateway	●					
IP PBX	●	●				
Gateways & IADs	●	●				
Video Conf/Transcoding	●					
Wireless Transcoding	●					
Video Transcoding	●					
Terminal Adaptor		●				●
Switch/Router						●
Home Gateway Triple Play			▲			
V2IP Phone/TV Out			▲	▲▲		
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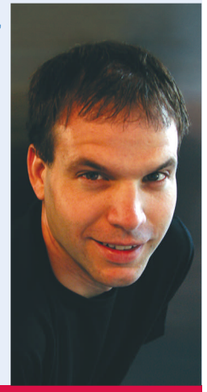

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Implementing Real-World Interfaces with FPGAs

This month, industry expert Nicholas Cravotta explores the key issues behind implementing interfaces in FPGA-based systems, including:

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- Weighing dis-integration options of components to improve overall cost/performance

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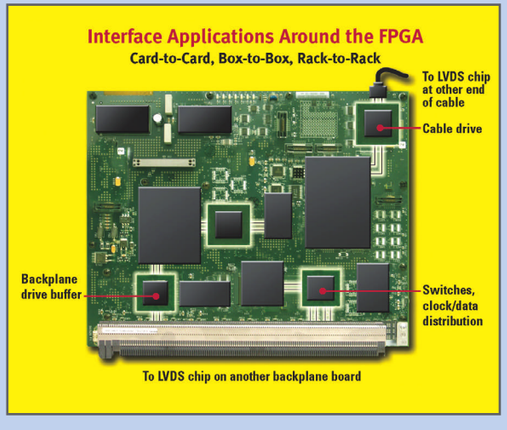
SCANSTA112	7-Port Multidrop IEEE 1149.1 (JTAG) Multiplexer	FBGA, TQFP, Evaluation Board	-40˚ C to 85˚ C
EQ50F100	1 Gbps - 6.25 Gbps Backplane Equalizer	Evaluation Board, LLP	-40˚ C to 85˚ C
DS90LV004	Four-Channel LVDS Repeaters with Pre-Emphasis	TQFP	-40˚ C to 85˚ C
SCAN90004	Four-Channel LVDS Repeaters with Pre-Emphasis and IEEE 1149.6	Evaluation Board, TQFP	-40˚ C to 85˚ C



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BY BONNIE BAKER

When undersampling, clock jitter *does* matter

In undersampling applications, such as wideband receivers, cellular base stations, and communications receivers, the undersampled signal has a relatively low-frequency bandwidth—with the help of the Nyquist Theorem and slower clocks to the converter. However, the carrier frequency for this signal frequency is high enough so that timing inconsistencies, such as clock jitter (or phase noise) and ADC aperture jitter, can increase noise as the signal goes through the ADC. Large amounts of jitter make the ADC block unusable for this type of system.

The noise sources in this type of application include the quantization noise of the converter (or the ac differential-nonlinearity error), the internal converter thermal noise, and the system jitter. The ADC quantization noise and thermal noise have a direct effect on the converter's SNR (signal-to-noise ratio), which is under your control only as you select the converter. The contributors to the system jitter are the aperture jitter of the sample-and-hold switch at the input of the ADC and the sampling-clock jitter. Aperture jitter is the sample-to-sample-variation timing of the ADC's input switch. The product data sheet indicates the aperture-jitter specification of your undersampling ADC. Clock jitter is an artifact of clock variation from cycle to cycle. You combine these two uncorrelated jitter-noise sources using the root-sum-square formula, or $t_{JITTER}=\sqrt{(t_{JCLOCK}^2+t_{JADC}^2)}$ in rms picoseconds, where t_{JITTER} is the total jitter of the system, t_{JCLOCK} is the jitter from the external ADC clock, and t_{JADC} is the jitter of the ADC-input-sampling switch. You cannot change your application circuit to improve the ADC's aperture jitter. However, several techniques can improve the clock jitter.

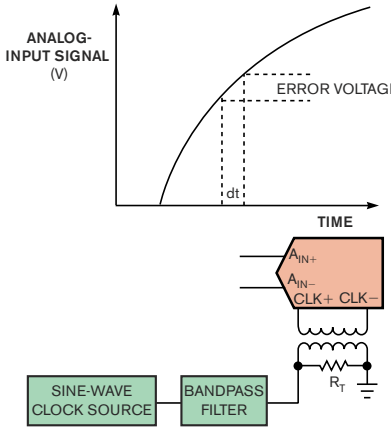


Figure 1 A variation of phase or jitter in the converter's clock input causes a deviation in the sampling time of the ADC-analog-input signal. This deviation produces degradation in conversion accuracy, which you quantify with the converter's SNR performance.

In this application, the external clock controls the sampling frequency or speed of successive conversions. Assuming the analog-input signal is void of phase shifts, clock jitter causes sampling-time uncertainty (**Figure 1**). This uncertainty affects the SNR of the conversion. The theoretical impact on SNR, due to jitter from the clock as well as from the ADC-sampling mechanism, is $SNR\ (dBc)=-20\log_{10}(2\pi f_{IN}t_{JITTER})$, where f_{IN} is the analog-input frequency.

Undersampling systems requires a clock with low jitter or phase noise to drive the ADC. These clocks can be digital or sinusoidal. Digital clocks have a fast slewing transition, which facilitates the reduction of clock jitter. However, the fast edges of digital clocks create wideband noise due to the complexity of the square wave's frequency content, producing wideband noise that aliases back into the signal bandwidth. Sinusoidal clock signals may be alternatives to the digital-clock option, depending on your application layout and implementation. However, they usually have higher rms near-band jitter. (Most ADC vendors provide clock recommendations for their converters.)

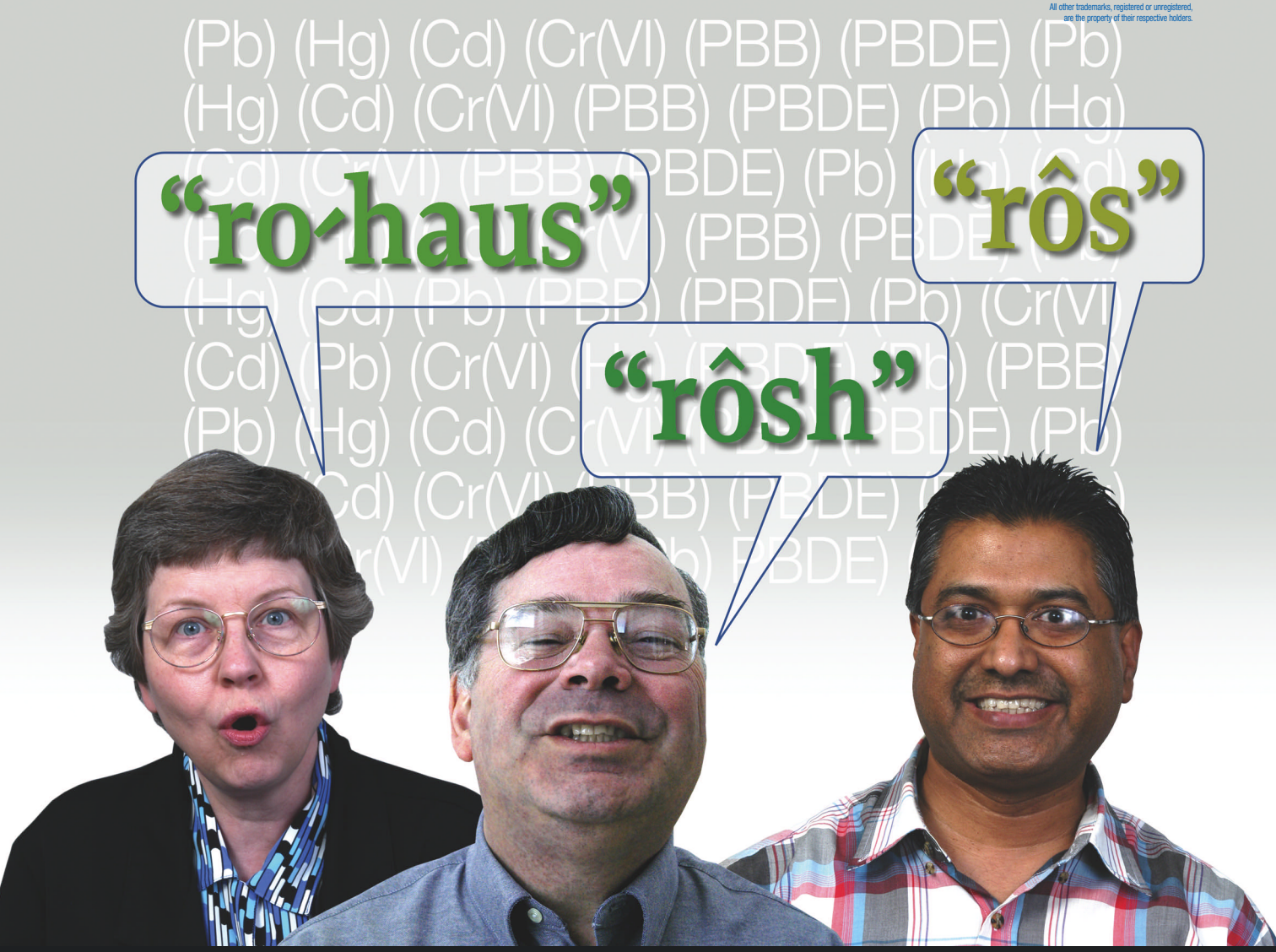
Using differential versus single-ended inputs is another clock alternative with most undersampling ADCs. Single-ended clocks must have a clock slope of approximately 1V/nsec or better. Single-ended inputs are not appropriate connections for sine-wave clocks. In addition, you need limits to the voltage swing of the single-ended clock. Otherwise, the clock signal bumps into supply rails, turning on internal protection devices. Differential-clock signals double the voltage range of the clock. The converter also does some common-mode rejection of noise signals.

So, when planning your clock strategy for your undersampling ADC, you should take into account your clock phase noise or jitter. The clock source you choose need not be expensive—only low noise. EDN

MORE AT EDN.COM

Go to www.edn.com/050804bb and click on Feedback Loop to post a comment on this column.

Bonnie Baker is the author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie.baker@microchip.com.*



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Go to www.edn.com/050804pe for more on our deconstruction of the CVS camera, including more pictures.

Cheap shot

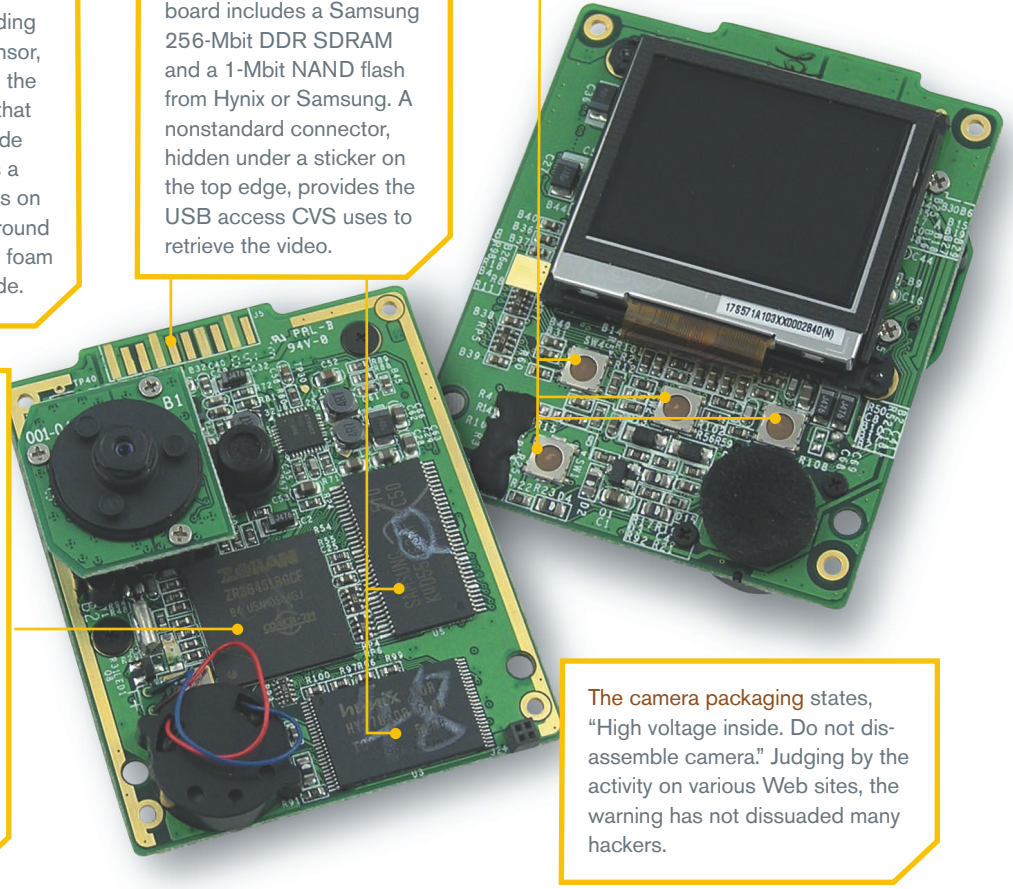
An SOC makes a one-time-use video camera feasible. Will consumers embrace the minimalist feature set?

Starting about a month ago, drugstore chain CVS began selling a digital-video camera for the paltry sum of $30. The product of digital-imaging specialists Pure Digital Technologies, the bare-bones device probably will serve most often in emergency roles—such as when dad forgets to charge the battery for the family camcorder. On the other hand, the camera is so simple to use that it could develop a fan base. The buyer shoots the 20 minutes of footage the camera can store, takes it to a CVS, pays an additional $13, and minutes later receives a DVD. But how can CVS sell the camera at such a cheap price? Our Prying Eyes staff didn't have to skip many lunches to buy one and find out.

The camera features a grand total of four user buttons: power, playback, record, and delete. The COACH's impressive autoconfiguration capabilities allow the camera to adapt to light levels, but for $30, don't expect focus and zoom.

The camera has no removable memory, but the board includes a Samsung 256-Mbit DDR SDRAM and a 1-Mbit NAND flash from Hynix or Samsung. A nonstandard connector, hidden under a sticker on the top edge, provides the USB access CVS uses to retrieve the video.

The bulk of the circuitry, including the digital chips, an image sensor, and a microphone, resides on the side of a 2.5×2-in. pc board that faces the subject (left). The side facing the videographer hosts a 1.4-in. LCD. A speaker mounts on the subject side, flush with a round hole in the board; an acoustic foam cover is visible on the LCD side.



Zoran's ZR36451 SOC, a member of the company's COACH (camera on a chip) 7 family, implements the digital portion of the design, except memory and the display. The SOC includes a 32-bit MIPS core, a display controller, a 480-Mbps USB interface, memory interfaces, and video-processing support. The chip, which includes DSP capabilities, handles 640×480-pixel (VGA) encoding at 30 fps using Zoran's TruDV compression technology.

The camera packaging states, "High voltage inside. Do not disassemble camera." Judging by the activity on various Web sites, the warning has not dissuaded many hackers.

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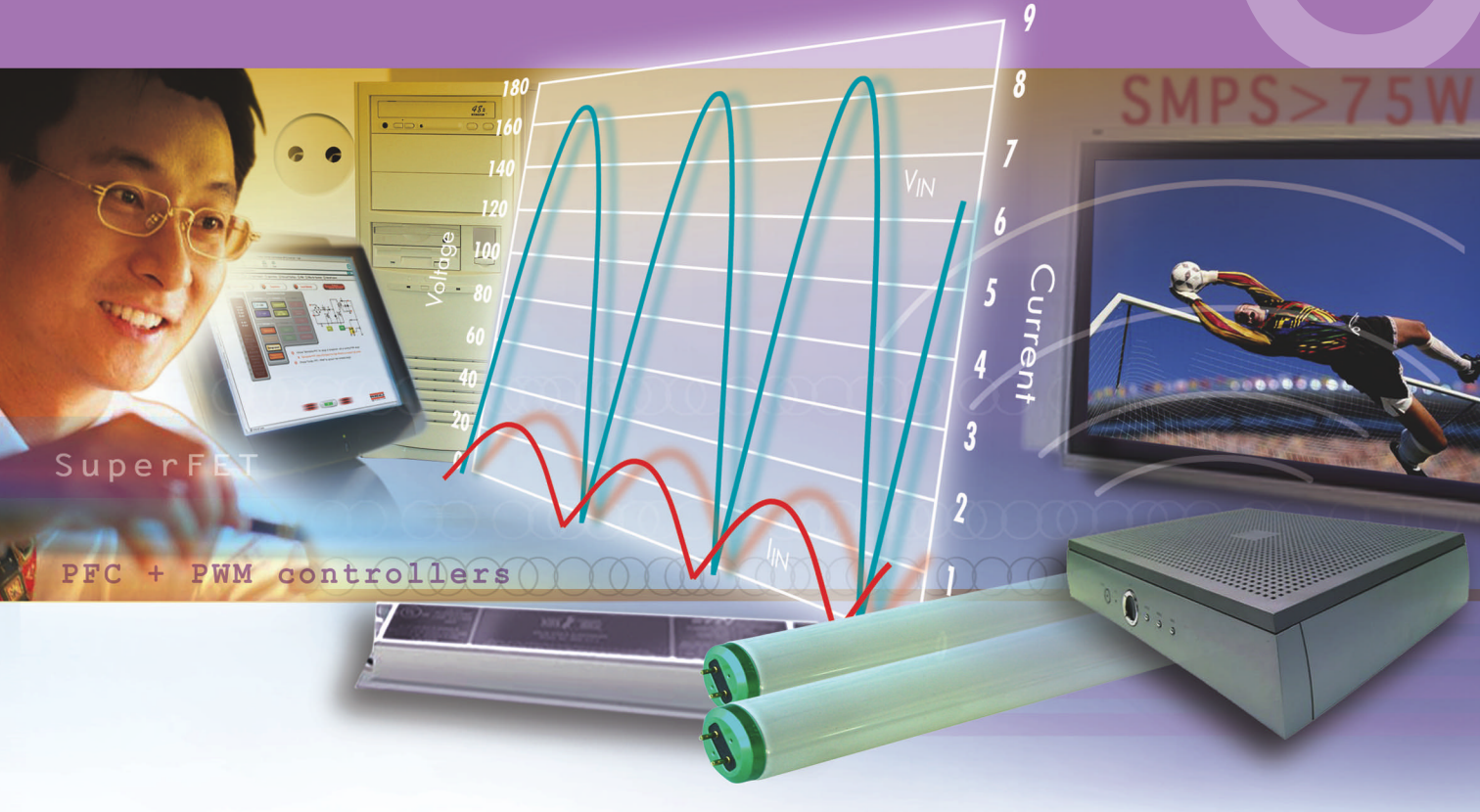

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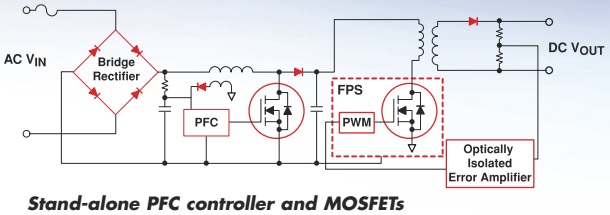
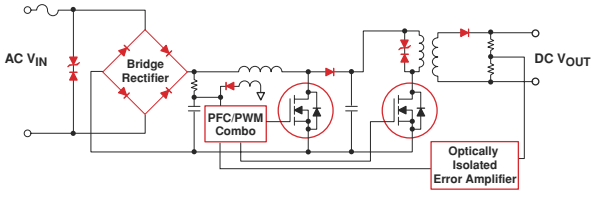


Stand-alone PFC controller and MOSFETs



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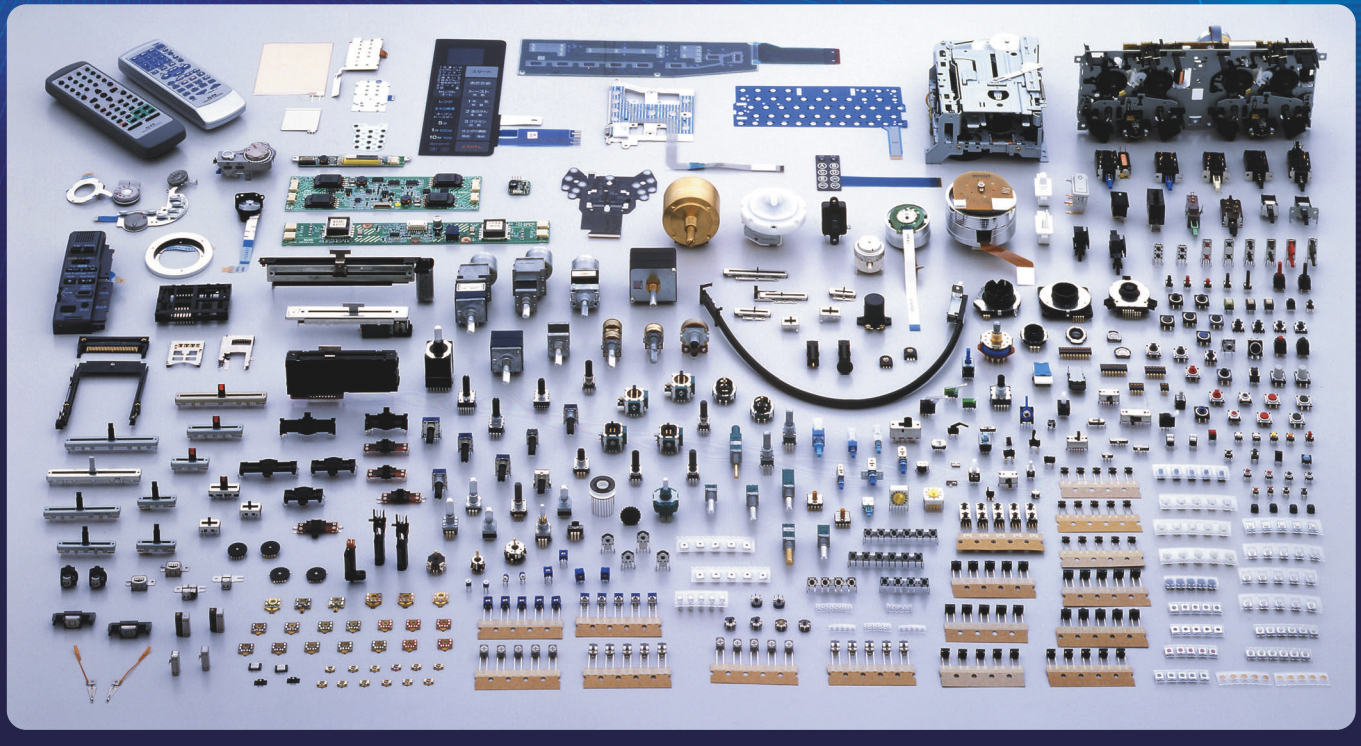

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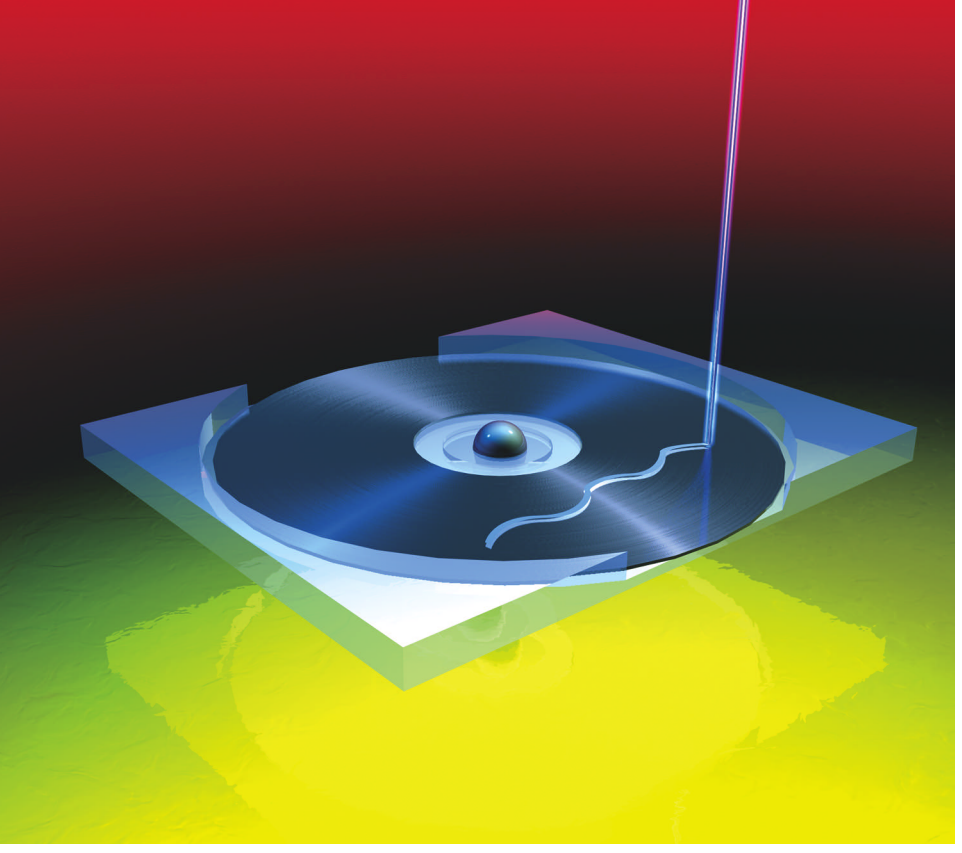

TECH TRENDS BRIAN DIPERT • SENIOR TECHNICAL EDITOR

Beating the blue-laser blues

CUSTOMERS WANT UNIFIED-FORMAT, BLUE-LASER-BASED STORAGE. DISREGARDING THOSE DESIRES, COMPETITORS ARE PUSHING BROADLY INCOMPATIBLE PRODUCTS INTO THE MARKET, IN A HIGH-STAKES GAME OF HIGH-TECH CHICKEN.

Industry standardization is a fickle mistress. Just ask the manufacturers of optical drives, their building blocks, and media. On the one hand, a unified technological approach to addressing a market need encourages broad industry-supplier support that reassures customers of the approach's viability and longevity, thereby encouraging them to open their wallets and make significant investments in it. On the other hand, unless that technological approach regularly evolves, encouraging those same customers to repeatedly *reopen* their wallets, the market stalls, and profits evaporate.

Looking at *EDN*'s last in-depth coverage of optical-storage technology two years ago, you might conclude that nothing's changed since (**references 1** and **2**). In a sense, you'd be right. Contending + and − writable- and rewritable-DVD formats still square off in the market. DVD-RAM is still a niche product that users employ in hard-disk-drive-emulating computer applications and that some manufacturers include in DVD recorders, PVRs (personal video recorders), and set-top boxes. Holographic storage still isn't in production. And the dueling Blu-ray and HD-DVD optical-storage alternatives are still staring each other down in an expensive face-off that, until resolved, threatens to stall the red-to-blue-laser-market transition.

It didn't need to be this way. "Those who cannot remember the past are condemned to repeat it," said US philosopher George Santayana in 1905. And more than 2000 years earlier, Chinese philosopher Confucius suggested that you "study the past if you would divine the future." What lessons does the past hold for today's storage pioneers? For starters, look at the Betamax-versus-VHS wars of the mid-1970s. Look at the saber-rattling and posturing that stretched out DVD-Video's gestation period to more than three or four years, depending on how you measure its endpoint: first products in the market in late 1997 or notable market success at the holiday-1998 shopping season (**Reference 3**). Or look at the +-versus-−-format wars, which only the widespread availability of format-agnostic universal players and recorders has subdued.

A NO-COMPROMISE QUAGMIRE

In February, it appeared that the Blu-ray and HD-DVD camps might in fact have learned their history lessons. Stung by widespread CES (Consumer Electronics Show) backlash to the two groups' significantly incompatible formats, they returned to the bargaining table in an attempt to hammer out a compromise. A settlement may occur, but, by press time, it didn't seem likely, with Sony Consumer Electronics President Ken Kutaragi commenting that negotiations are "game over," the Blu-ray-inclusive Playstation 3 launch slated for next spring, and Toshiba President Tadashi Okamura's stating, "We may actually have a situation where merchandise from both sides are put on store shelves. But the market would not allow that situation to last very long" (**references 4** and **5**).

Blu-ray backers continue to tout their revolutionary technology's superior per-layer storage capacity of 25 Gbytes. HD-DVD advocates counter that their evolutionary approach's 15-Gbyte/layer capacity is good enough, especially when you consider it in the context of the me-

AT A GLANCE

- An inability to compromise and blend their respective patent portfolios leaves the two blue-laser-consumer-storage camps facing an uncertain future.
- Advanced video codecs let you store high-resolution, long-playing movies on mainstream red-laser-DVD media.
- The red-laser-optical industry hopes to extend its relevance through multilayer and dual-sided storage, higher write speeds, and dimensional diversity.
- After years of research and development and plenty of unrealized expectations, holographic storage may finally enter the market next year.

Figure 1 Both HD-DVD proponents and their Blu-ray competitors are gearing up for production (a, courtesy Maxell), but multiformat confusion and a prevalence of advanced video codecs that can deliver high-resolution, full-length movies on red-laser media may dash their near-term plans (b, courtesy JVC).

dia's compatibility with today's DVDs, which they believe will speed and minimize the cost of the conversion of optical-disc manufacturing lines to the next-generation technology. Late May's Media-Tech Expo conference in Las Vegas was the scene of numerous dueling press releases: Toshiba unveiled a three-layer 45-Gbyte HD DVD that neared its competitor's two-layer capacity, and Blu-ray backer TDK responded with a four-layer, 100-Gbyte prototype. Less than three weeks later, Hitachi-Maxell and Verbatim announced their mass-production mastery of a write-once, 15-Gbyte HD DVD-R (**Figure 1a**). This summer's tit for tat comes on the heels of last December's announcement by Toshiba and Memory-Tech of dual-layer media that users can play on both conventional-DVD and next-generation HD-DVD players, enabling them, for example, to watch a movie in standard definition on a legacy player and in high definition on a new HD-DVD player. That announcement provoked a response, again less than three weeks later, by JVC, which unveiled a 33.5-Gbyte disk that combines a 25-Gbyte Blu-ray layer and an 8.5-Gbyte dual-DVD layer.

All of this next-generation debate focuses on the consumer market. Blue-laser-based optical storage is *already* in production, albeit targeting high-end applications. TDK, for example, is shipping a 23.3-Gbyte cartridge touting a 72-Mbps-per-head transfer rate, for use in Sony's XDCAM Professional Disc system. Verbatim, conversely, is shipping 30-Gbyte UDO (ultra-density-optical) media, primarily for use in optical libraries, and professional desktop systems for legal, financial, health-care, and government applications, according to Optical Storage Manager Tim Clatterbuck. Hewlett-Packard and Plasmon, along with Sony,

DATA LONGEVITY

How long will the information stored on an optical disc remain intact? This frequently asked question came to the forefront when the first CD-Rs appeared on the market, and users have been asking it ever since. (Pressed CDs and DVDs permanently retain their contents, as long as you don't break or otherwise mar them.) Potential variables include the write- and read-back speeds, the characteristics of the drive accessing the media, the physical makeup of the media itself, and the ambient conditions under which users write, store, and subsequently access information. The NIST (National Institute of Standards and Technology) has published the preliminary results of a study to answer this question. The samples are small, so the data's statistically unsound, but it still makes for interesting reading. Check it out in PDF format on the NIST Web site; you can also peruse the ensuing Slashdot debate (references A and B).

REFERENCES

A Slattery, Oliver, Richang Lu, Jian Zheng, Fred Byers, and Xiao Tang, "Stability Comparison of Recordable Optical Discs–A Study of Error Rates in Harsh Conditions," *Journal of Research of the National Institute of Standards and Technology, Volume 109, No. 5*, September to October 2004, www.itl.nist.gov/div895/gipwg/StabilityStudy.pdf.

B "NIST releases study of CD/DVD longevity," http://hardware.slashdot.org/article.pl?sid=05/02/05/0024258.

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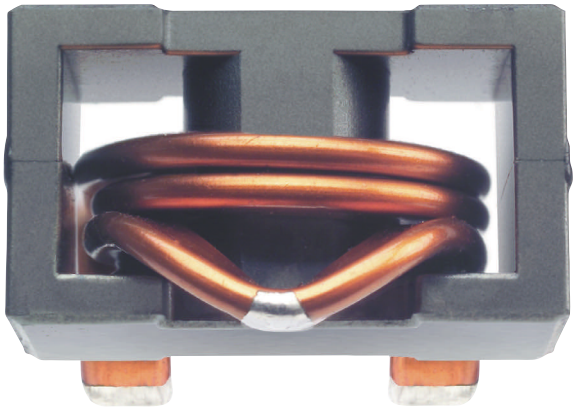

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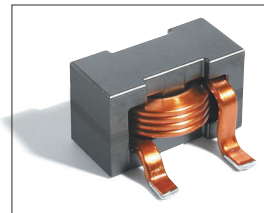

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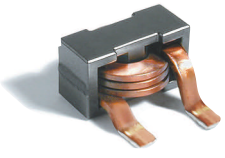

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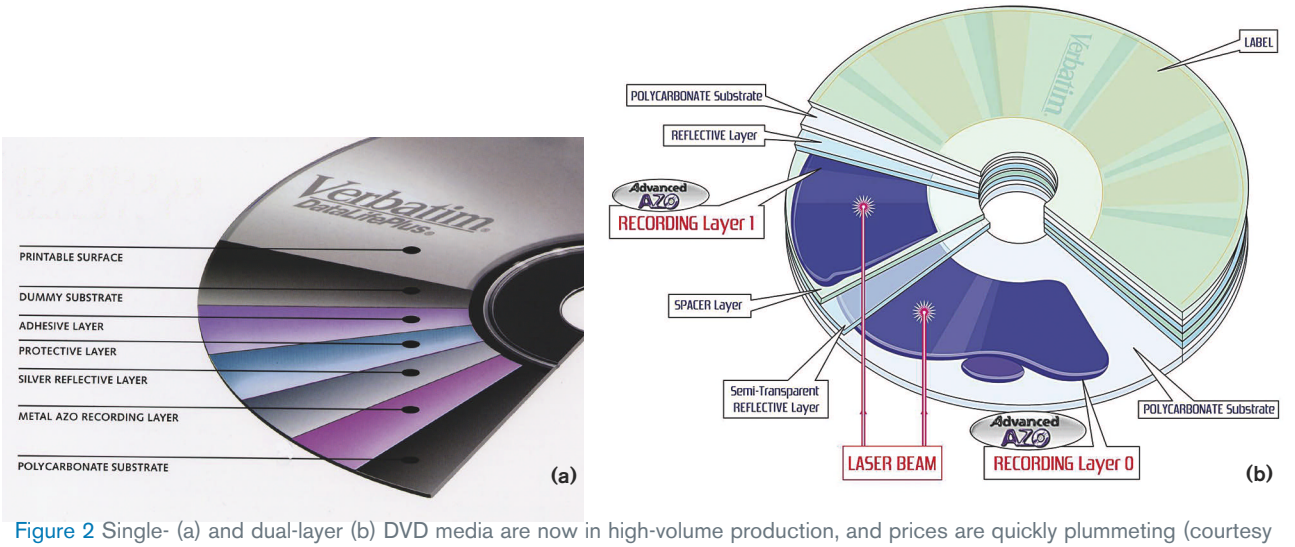

Figure 2 Single- (a) and dual-layer (b) DVD media are now in high-volume production, and prices are quickly plummeting (courtesy Verbatim).

developed UDO; Sony later backed out to focus on Blu-ray. The Ecma International, ISO (International Standards Organization), and IEC (International Electrotechnical Commission) standards bodies have approved UDO. Clatterbuck claims, "Write-once UDO media has a data life of 50 years. For work in progress or files that need to be updated, the Verbatim rewritable UDO media delivers more than 10,000 direct-overwrite cycles" (see **sidebar** "Data longevity"). Verbatim also claims that next-generation 60- (single-sided) and 120-Gbyte (double-sided) UDO media is under development.

With DVD history as a guide to future trends, video capture and playback will likely be the dominant applications of next-generation blue-laser optical media, at least in its early life. Sonic Solutions, which recently acquired Roxio—along with competitors such as CyberLink, InterVideo and Ulead, and NTI Software—is busy preparing next-generation software, for both consumers and professional users, that works with next-generation optical media, its relevant audio and video codecs, and its DRM (digital-rights-management) schemes. Jim Taylor, the maintainer of the DVD Forum's FAQ, author of *DVD Demystified*, and general manager of the Advanced Technology Group at Sonic Solutions, states, "At the consumer-content-creation level, lack of unification," resulting from the looming conflict between Blu-ray and HD DVD and the resultant potential for customer confusion, "won't have a big effect" on his company's fortunes.

The capacities of Blu-ray and HD DVD, however, represent overkill for the standard-definition-resolution images that today's miniDV camcorders produce, and next-generation HDV camcorders haven't yet dipped below the $1000 price barrier. Forecasting the near-term impact of format confusion on the high-definition-prerecorded-movie market and therefore the market for Sonic's professional tool sets, Taylor says, "Content creators will move ahead with whatever format they choose." Much of the fuel for his optimism is that hardware suppliers are highly motivated to sell new equipment to consumers, as well as to establish their anointed format as the de facto industry standard, and will therefore aggressively push abundant supply and low prices.

BLUE-LASER STALL

Taylor's predictions about blue-laser technology, however, are curiously at odds with the multiple market slowdowns that DVD has experienced in the face of format wars. Taking off his Sonic hat, Taylor says, "If there is format confusion, if both stay in the market for a year or so, there will inevitably be dual-playback devices. The format groups themselves have studiously avoided any discussion of universal players. But, looking at historical developments, companies will figure out how to support consumers across multiple formats. License and patent royalties are a factor. The main technical issue, which can be solved, is that there has to be CD playback—not mandatory but de facto—meaning that there are three levels that the laser needs to focus on." Taylor refers to the 1.2-mm level for CDs, the 0.6-mm level for DVDs and HD DVDs, and the 0.1-mm level for Blu-ray. "The pickup head must be able to handle that, plus it must comprehend multiple wavelengths: infrared for CD, red for DVD, and two blue wavelengths to deal with both HD DVD and Blu-ray. It's not practical now, especially with slim drives in notebooks. But it will be cost-effective within one to two years," predicts Taylor.

He also believes that, in case of format confusion and until that confusion settles

HANDS-ON PLANS

***EDN* will encode high-resolution video clips–both from industry contacts and personally captured with a 720p JVC HDV camcorder–to DivX 6, MPEG-4 AVC, WMV9, and other leading-edge video formats, burn them onto DVD-Rs and DVD+Rs, and compare the results, thereby exploring the premise of whether blue laser's slowdown will mean an extension of red laser's longevity (references A and B). Visit the Brian's Brain blog at www.edn.com/briansbrain for the rest of the story.**

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A Dipert, Brian, "Video characterization creates hands-on headaches," *EDN*, July 25, 2002, pg 53.

B Dipert, Brian, "Video characterization creates hands-on headaches: part two," *EDN*, Aug 8, 2002, pg 81.

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down, "there will be a window of opportunity for red-laser-based HD formats to do better than they would otherwise" (see **sidebar** "Hands-on plans"). The movie studios, after all, are eager to encourage consumers to buy high-definition variants of content they already own on DVD and to buy more expensive HD versions of content they don't yet own, but they're uncomfortable with the prospect of selecting—and possibly incorrectly selecting—one of the two dueling blue-laser formats. Alternatively, they face the equally unappealing prospect of having to support both formats. They also don't like the prospect of advocating that consumers buy expensive next-generation players that might not handle other studios' material.

Figure 3 Nintendo's GameCube (a) and Sony's Playstation Portable (b) employ smaller-than-standard red-laser-media dimensions as one means of copy protection.

Audio- and video-codec developers are poised to exploit this window of opportunity. Microsoft has for several years offered DVDs that contain high-resolution movie variants in Windows Media Video 9, or VC-1, format, in conjunction with studio partners such as Artisan and Imax. In June, DivX released Version 6 of its MPEG-4 Advanced Simple Profile-derived video codec, which supports interactive video menus, chapters, subtitles, alternate audio tracks, and video tags. DivX claims that the Version 6 codec has a 20 to 40% quality and bit-rate improvement over that of Version 5. And most notably for this discussion, lead DivX codec engineer Jerome Rota states, "Most 720p [720-line-progressive-scan] content requires only a 4-Mbps average bit rate, whereas 1080p content demands only 6 to 8 Mbps." These bit rates are on par with today's 480-line, standard-definition DVD bit rate using MPEG-2.

Nero (formerly, Ahead Software) and partner Ateme are aggressively promoting Nero Digital, an extension-based enhancement of MPEG-4 AVC (also known as MPEG-4 Part 10, or H.264). Nero, like DivX, has also branded a proprietary spin of the MPEG-4 Advanced Simple profile, albeit in this case with an MPEG-4-approved AAC (Advanced Audio Compression) audio codec and "wrapper." Udo Eberlein, president of the company's US subsidiary, is bullish on MPEG-4 AVC's ability to beat DivX 6 on a quality-versus-bit-rate basis and to more than hold its own against the Microsoft VC-1 counterpart, as well. Eberlein admits that, whereas VC-1's Advanced Profile is available, MPEG-4 AVC's high profile is not yet released. "Currently, VC-1 is more mature in the professional-tools space," he acknowledges, and, for that reason and others, Warner Brothers, for example, will likely encode its first wave of HD DVDs using VC-1. "In the consumer-tools space, however, Nero has been shipping MPEG-4 AVC since December 2004 in Nero Version 6.6," he points out. Nero has also developed audio- and video-decoder hardware IP (intellectual property) that it offers for license to potential semiconductor and systems partners.

DVD hardware can now exploit this window of opportunity. Players from Buffalo and I-O Data support one or more of these advanced codecs, and JVC and V Inc will soon follow (**Figure 1b**). However, the current generation of players lacks support for the necessary authorization DRM scheme for the WMV (Windows Media Video) HD DVDs, meaning that you need to play them on either a conventional or a Media Center Edition PC. To that point: Most consumers will likely need to buy a new player to experience any of these new video codecs and their associated audio codecs, DRM schemes, and wrapper formats in their living rooms. However, this new player will, at least initially, be much less expensive than a blue-laser-based alternative. And here's the key: Anyone with a DVD-ROM drive in his PC can install the necessary software and today experience high-definition content.

How big is the window of opportunity? Taylor, again speaking for himself and not for his company, comments, "Having been through one [the original DVD-video] format launch, there are likely to be delays, and I doubt anything will be out by year-end from either camp." Several industry representatives spoke off the record, saying that they expect that the HD-DVD group will come to market in the first quarter of next year and that Blu-ray, with Playstation 3 in the lead, will follow in the second quarter. And will one of the two format camps eventually throw in the towel and yield to the competition—and, if so, when? That's anyone's guess.

Other countries have also seen the wisdom of a red-laser-based, high-definition-video approach. China's EVD (Enhanced Versatile Disc), as its developers originally defined it, employed On2 Technology's VP5 and VP6 video codecs, along with Coding Technologies' six-channel EAC (enhanced audio codec). One of the primary motivations for EVD was to dodge expensive royalty payments to MPEG-2, CSS (content-scrambling-system), and Macrovision analog-copy-protection rights holders, although, in an apparent contradiction, EVD backers claimed that players would also support DVDs. EVD supported 720p and 1080i video resolutions and was also backward-compatible with CD, VCD (video CD), and SVCD (super VCD). However, ini-

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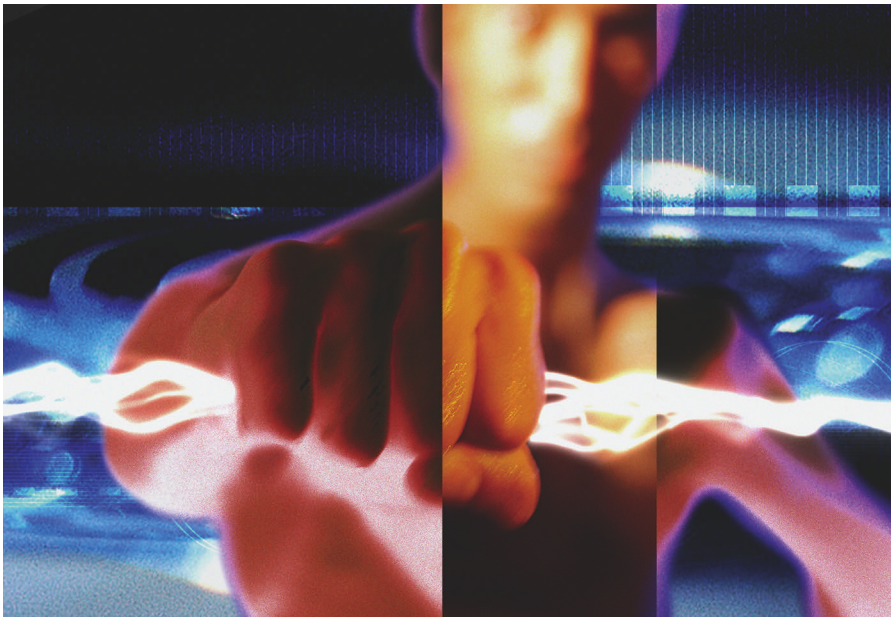

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SP3072E	1Tx/1Rx	half	250kbps	±15kV	8 Pin NSOIC
SP3073E	1Tx/1Rx	full	500kbps	±15kV	14 Pin NSOIC
SP3074E	1Tx/1Rx	full	500kbps	±15kV	8 Pin NSOIC
SP3075E	1Tx/1Rx	half	500kbps	±15kV	8 Pin NSOIC
SP3076E	1Tx/1Rx	full	16Mbps	±15kV	14 Pin NSOIC
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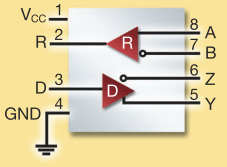
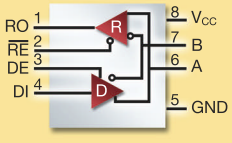
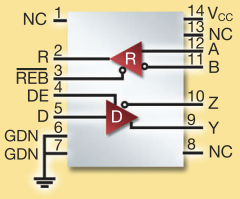


8 Pin Half Duplex



14 Pin Full Duplex



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tial product demos employed LSI Logic-supplied high-definition MPEG-2, and a dispute early last year between On2 and EVD developers may have permanently sidelined the format, although a video-codec conversion to AVS (advanced video coding standard in information technology) is also a possibility (**Reference 6**).

Taiwan's Opto-Electronics and Systems Laboratories, under the government-sponsored Industrial Technology Research Institute, has similarly developed the FVD (forward versatile disc), which employs Microsoft's WMA (Windows Media Audio) Professional codec and WMV codec, albeit with hardware-based AES (Advanced Encryption System) decryption instead of Microsoft's DRM scheme. FVD differs from the DVD standard in physical format: First-generation FVD discs have 5.4- to 6-Gbyte, single-sided and 9.8- to 11-Gbyte, double-sided storage capacities and support resolutions as high as 1280×720 pixels in progressive-scan mode. Second-generation FVD discs, with a capacity of more than 15 Gbytes, will support resolutions as high as 1920×1080 pixels in interlaced mode.

EVOLUTION, DIVERSIFICATION

The data on the DealNews and Techbargains sites at press time would elate consumers and depress suppliers. A 100-CD-R pack of name-brand 52× devices was selling for $12, including shipping and after rebate. That price translates to 17 cents per gigabyte. Even more incredible, a 100-unit pack of name-brand 8× DVD-Rs or DVD+Rs was going for $20, translating to just over 4 cents per gigabyte. Brand-new, 16×, dual-layer-capable burners sell for less than $50, and, in June, you could buy refurbished Pioneer DVR-109s for $37.50 each. New 52× CD burners sell for $20. And DVD players are free after rebate.

Although media and drive suppliers eagerly await the salvation that blue-laser discs promise, they're in the near term tweaking red-laser technology wherever they can in the hope of eking out a profit. Dual-layer writing capability was a nebulous forecast when *EDN* last published an optical-storage article (**Figure 2**), but it's now here, at 8× speeds for DVD+R media and 4× rates for DVD-R, judging from recent drive announcements by companies such as Plextor. (These announcements reflect a more general historical trend of + media's achieving performance thresholds before the − alternatives, which eventually match those thresholds.) Although dual-layer-capable drives are dirt-cheap, the media—now supporting only 2.4× write speeds—is comparatively expensive, currently selling for around $5 per blank disc.

In June, single-layer media capable of a 16× write rate was also roughly twice as expensive as 4 and 8× counterparts; the price difference may have disappeared by now. DVD+RW has even hit 16× speeds, with DVD-RW close behind it at 12×. As is the case with the aforementioned dual-layer DVD, drive specifications may tout high-speed support, but commercially available media cannot yet handle these extreme write rates. And don't expect even faster performance in the future; a 16× DVD-rotational speed roughly correlates to the speed of a 52× CD, which is the speed at which that technology topped out. As was the case in the CD-to-DVD transition, blue-laser-based technologies will likely increase the drive- and media-transfer rates by storing more data in the same amount of space, instead of spinning the disk faster.

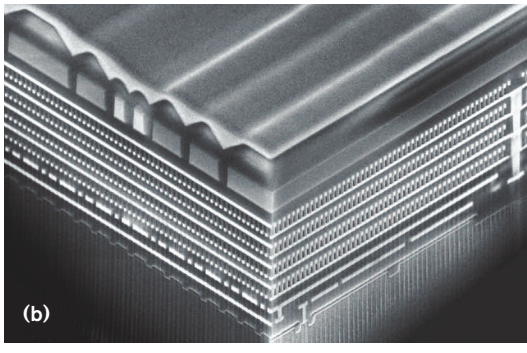

Figure 4 By varying the reference beam angle, wavelength, and media position, InPhase Technologies lets you record many holograms in and read them back from the same volume of optical material with the added potential for data security using custom laser wavelengths and drive-specific phase masks. The company slates 300-Gbyte, first-generation drives and media for production next year (a). Meanwhile, semiconductor storage is making capacity leaps and bounds of its own (b, courtesy Matrix Semiconductor).

DVD-Audio and SACD (Super Audio CD) have been underwhelming market performers; most audio listeners don't appear to be enthralled with high-resolution audio and surround sound (**references 7** through **9**). Or perhaps consumers are just unwilling to pay the incremental price necessary to obtain these features, especially considering that CD-quality, two-channel audio is available for "free" on peer-to-peer file-sharing networks and is nearly free on offshore music-distribution sites, such as Allofmp3. To that point: The music labels are desperate to hook listeners onto again buying music, and the DualDisc is their latest tack. This dual-format disc contains an audio CD layer on one side and SACD, DVD-Audio, or DVD-Video media on the other. Initial consumer response seems to be generally positive; the fact that prices are comparable with the CD-only alternative doesn't hurt. DualDisc's most notable issue is its greater thickness—1.5 mm—compared with an average-sized, 1.2-mm CD or DVD, which means that it doesn't fit in some players. The CD side of a DualDisc is also restricted to 60 minutes of capacity. (Red Book Audio CDs hold as much as 74 min-

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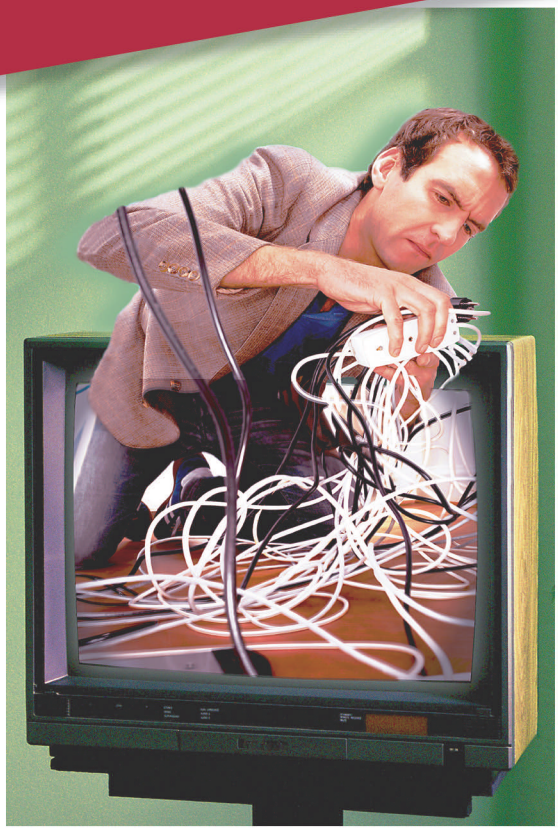

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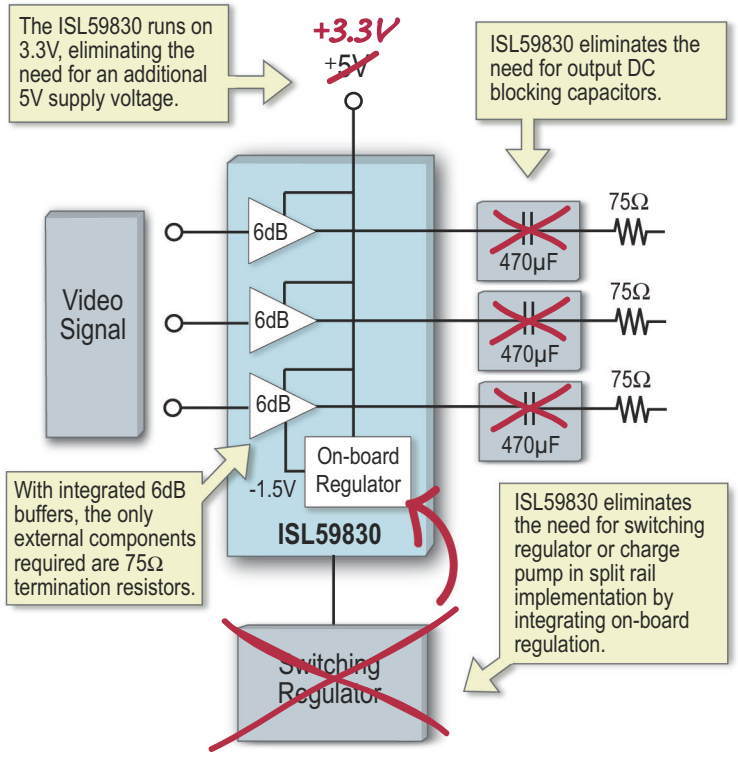
ISL59830 Functional Block Diagram



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utes of content.) Also, the DVD side cannot contain more than one layer's worth of data, again to keep thickness at a generally manageable level.

Microsoft's Xbox and Sony's Playstation 2 employ otherwise-conventional CD and DVD media, containing copy-protected data that users can circumvent only by using "mod chips" (devices that let users circumvent the DRM of a game console) or by otherwise exploiting vulnerabilities in the operating system and applications (**Reference 10**). Nintendo's GameCube takes duplication prevention to the next level of complexity; it employs a proprietary, 80-mm (approximately 3.2-in.-diameter), red-laser-based optical disc that stores 1.5 Gbytes of information. The drive accesses this information beginning at the disc's outer edge, whereas conventional optical-disc accesses begin at the inner edge (**Figure 3**). The Sony PSP's (Playstation Portable's) 60-mm (approximately 2.4-in.-diameter), red-laser-based and 128-bit AES-encrypted, 1.8-Gbyte UMD (Universal Media Disc) targets use in both games and feature-length movies and is similarly proprietary in format. In June, Sony was striving to stay one firmware release ahead of hackers, who have so far figured out how to copy UMD data to a MemoryStick Duo and run games from that flash-memory-based media (**Reference 11**).

Three primary means exist for squeezing more data onto a given-sized piece of CD media: narrowing the track-to-track pitch, reducing the within-track spacing between pits and lands, and extending the total available track length. Industry-specification-contravening technologies exploit these techniques to shoehorn more information onto a CD. These techniques include various suppliers' 790- and 870-Mbyte discs, Plextor's GigaRec, and Sanyo's HD-Burn, none of which the industry has widely adopted. Prodisc Technology has resurrected the capacity-boosting aspiration with a DVD twist. The company's 4.9-Gbyte DVD-R, introduced at the late-May Computex show, stores 200 Mbytes' worth of additional information by tightening the track-to-track pitch, but, at the time of its unveiling, it was fully compatible with only 15 drives and players; 100 more computer drives and 26 consumer DVD-R video recorders offer partial support, such as storage of as much as 4.7 Gbytes or lower recording speeds.

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What happens if two layers' worth of DVD storage capacity is insufficient, and you don't want to switch to any of the professional blue-laser formats or wait for Blu-ray or HD-DVD? Then, you might want to give New Medium Enterprises a call; the company claims that by year-end it will be shipping media and players compatible with its four-layer, 20-Gbyte red-laser VMD (Versatile Multilayer Disc) technology. The VMD red laser's future extends to 20 layers' worth of information at 5 Gbytes per layer, for a total capacity of 100 Gbytes. The company asserts that VMD-based drives will be able to read other standard formats, including CD and DVD. And the company's Web site also points out that "VMD multilayer technology does not strictly function with red laser only, but can easily be applied to blue laser as well." But will Hollywood bite? It's doubtful, but you'll have to see. You could ask the same question of EVD and FVD, and the question is particularly relevant given the notably inconsistent prosecution of media piracy in the parts of the world where proponents are advocating those formats.

Finally, because the laser is available to store information on the data side of a CD or DVD, why not also put it to good use on the other side? HP's LightScribe technology employs specially coated discs and enhanced disc-burning software to produce laser-etched labels. The LightScribe Web site lists BenQ, HP, LaCie, and Sager as hardware adoptees; Cyberlink, InterVideo, Nero, and Sonic as software implementers; and HP, Imation, Memorex, and Verbatim as media suppliers. LightScribe's capabilities are intriguing, but the FAQ document on the LightScribe Web site admits that drive and media supply is currently spotty. Unless availability dramatically improves, including an increase in the number of hardware and media providers, and costs consequently decrease to be more in line with alternatives, most folks will likely stick with the established ink-jet-printer-generated-label approach.

BLOG GOODIES

Holographic storage from InPhase Technologies and the Optware-chaired HVD (Holographic Versatile Disc) Alliance made a big splash at this year's CES and NAB (National Association of Broadcasters) conferences (**Figure 4**). InPhase demonstrated 200-Gbps/in.^{2} storage capacity at the NAB show and hopes to be in production by next year with first-generation 300-Gbyte, 20-Mbyte/sec recordable drives and media, with plans for a 1.6-Tbyte capacity and 120-Mbyte/sec access speeds by 2009. Other plans include 40-Mbyte/sec "ROM" media and 80-Mbyte/sec rewritable media, both with 1-Tbyte capacities by the decade's end.

For those yearning for faster accesses and less restrictive write capabilities, hard drives are also experiencing a significant capacity boost courtesy of the perpendicular-storage technique. And don't forget about semiconductors for the ultimate in read speeds; Matrix Semiconductor's latest Trinity 3-D memory squeezes 1 Gbit of storage into a four-layer, 31-mm^2 piece of silicon fabricated on a 0.15-micron-process technology, although, like CD-R, DVD-R, and DVD+R, it's a write-once technology. EDN

ACKNOWLEDGMENTS

Kudos to optical-storage-press-relations representative Andy Marken for connecting me with a diverse collection of vendors and for providing a plethora of research materials for this story.

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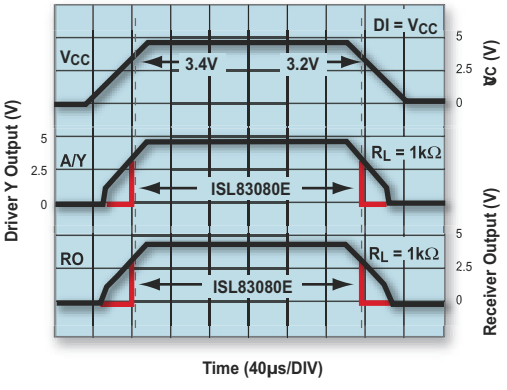

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Device	# of Tx/ # of Rx	Devices Allowed on Bus	Half/ Full Duplex	High ESD?	Hot Plug?	Data Rate (Mbps)	Slew Rate Limited?	Tx/Rx Enable?	ICC EN / DIS (µA)	SHDN ICC (µA)	VCC Range (+V)	Pkg.
ISL83080E	1 / 1	256	Full	Yes	Yes	0.115	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83082E	1 / 1	256	Half	Yes	Yes	0.115	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83083E	1 / 1	256	Full	Yes	Yes	0.5	Yes	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83085E	1 / 1	256	Half	Yes	Yes	0.5	Yes	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC
ISL83086E	1 / 1	256	Full	Yes	No	10	No	Yes	530 / 530	0.07	4.5 to 5.5	14 Ld SOIC
ISL83088E	1 / 1	256	Half	Yes	No	10	No	Yes	560 / 530	0.07	4.5 to 5.5	8 Ld MSOP 8 Ld SOIC

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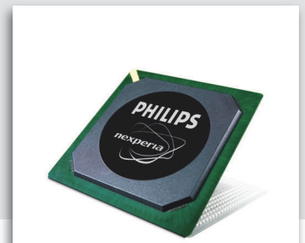

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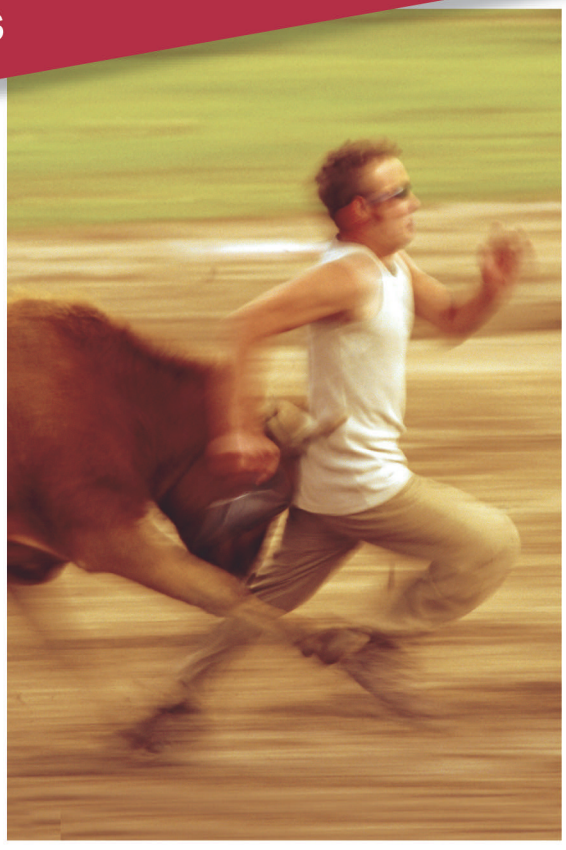

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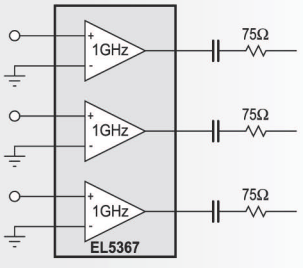

Part No.	BW (MHz)	SR (V/µs)	Is (mA)	Av (min) (V)	IOUT (mA)	VOUT (V)
EL5360	200	1700	0.75	1	70	±3.4
EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
EL5367	1000	6000	8.5	1	160	±3.8

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- 1.4GHz bandwidth
- 6000V/µs slew rate
- Less than 9mA power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	Is (mA)	Av (min) (V)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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- Virtually unlimited slew rate
- 700MHz gain of 1 bandwidth
- Almost zero overshoot
- Low power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	VN (nV/√ Hz)	Is (mA)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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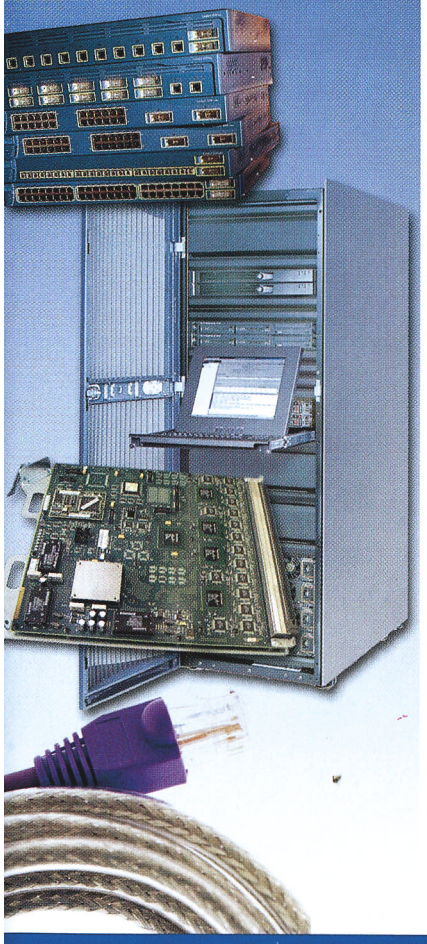


Analyzing Power Modules

— By Ramesh Khanna, Principal Applications Engineer

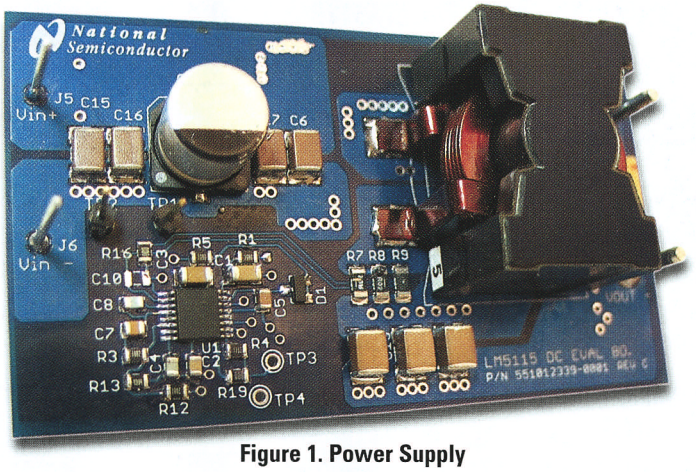


Figure 1. Power Supply

Power modules are supplies that are mounted directly on the PCB to power ASICs, DSPs, microprocessors, memory, FPGAs, and other digital or analog loads *(see Figure 1)*. These modules are commonly referred to as point of load supplies (POL) or point of use-power supplies (PUPS). Modules are extremely popular in high-performance telecommunication, networking, and data communications systems as they provide a number of benefits to a system. Despite these advantages, several reliability and measurement issues are often overlooked in most on board dc-dc converter designs as well as in power modules. This article will examine and address these issues.

Advantages of Using Power-Supply Modules

A variety of power modules in a combination of input voltages, output power levels, feature sets, topologies etc. are available from several vendors. Relative to down solutions, power modules reduce time-to-market. Other advantages are listed below.

- Every module can be thoroughly tested to ensure high reliability, including burn-in to weed out infant mortality. Conversely, the testing of a down solution is rather difficult as it is integrated with other solutions on the board.
- Multiple vendors can design a module with the same form factor, using one of several existing standards, thus providing the system engineer with alternative sources for his power needs.

NEXT ISSUE:

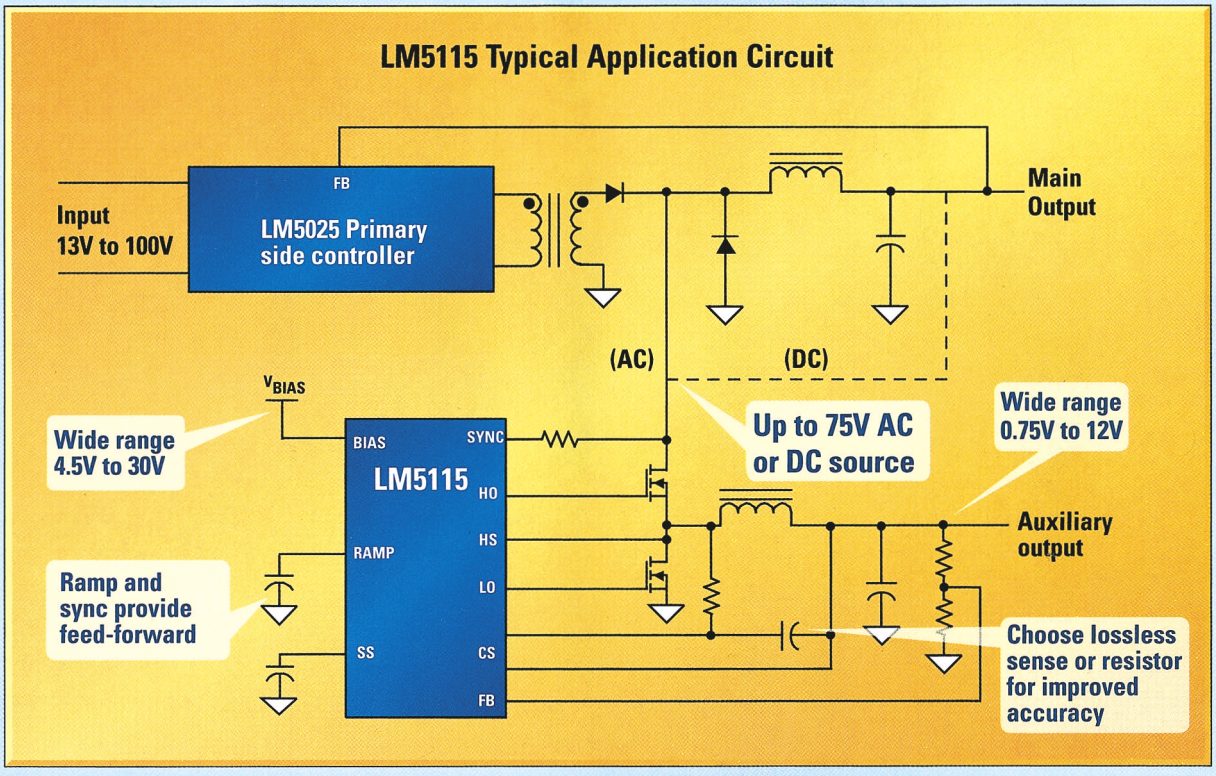
Active Clamp Power Converters

National Semiconductor

The Sight & Sound of Information

Secondary-Side Post Regulator (SSPR)

Feature-Rich LM5115 Controller Simplifies Design of Multiple Output DC-DC Converters and Doubles as High-Voltage DC-DC Controller



LM5115 Features

- Provides multiple outputs from main DC-DC or AC-DC converter
- Operates directly from secondary-side phase signal or DC input
- Leading-edge modulation for SSPR from current-mode primary controller
- Up to 1 MHz switching frequency reduces component footprint and profile
- Integrated gate drivers with 2.5A peak output current
- Available in TSSOP-16 and tiny LLP-16 packaging

Ideal for use as a secondary-side post regulator in the design of multiple output AC-DC or DC-DC power supplies or as a DC-DC controller for use in point-of-load (POL) regulators

Product Highlight:

Widest input range, high performance controller addresses diverse applications

Analyzing Power Modules

- Technical risks are minimized as each module is designed and tested to meet standardized performance requirements.
- The entire motherboard must be replaced if the down solution fails, whereas in the case of a module, the individual module can be replaced, saving cost and time.

Issues Often Overlooked While Designing Power Modules

Despite the advantages of modules highlighted above, a number of issues are often inadequately characterized or measured in module design (as well as in on-board dc-dc converter designs). These issues are:

- Output noise measurement
- Magnetics design
- Shoot-through in synchronous buck converters
- PCB reliability

These issues are examined in this article, with simple techniques for addressing them.

Output Noise Measurement Techniques

All switch mode power supplies generate output noise. As switching frequencies increase, it is becoming more critical to use proper measurement techniques to ensure that measured data are accurate and reliable. Using a Tektronix probe tip (often referred to as a cold-nose probe) for output noise and other critical measurements provides reliable and predictable measurements as shown in *Figure 2*. This measurement technique ensures that the ground loop is minimized.

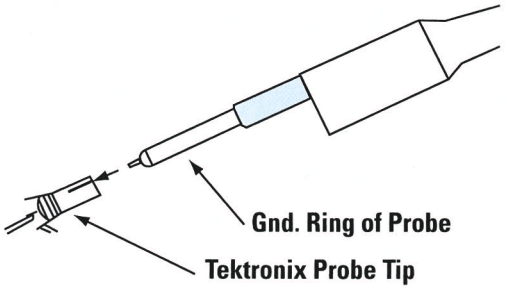


Figure 2. Output Noise Measurement

Another factor to consider when making measurements is that test instruments have propagation delays. Most current probes have greater propagation delays than voltage probes. Consequently measurements that require both voltage and current waveforms simultaneously cannot be done accurately unless the unequal delays are manually equalized.

Current probes also introduce inductance into the circuit. A typical current probe will introduce 600 nH of inductance. Thus in high-frequency designs where the desired circuit inductances can be 1µH or lower, the probe inductance will introduce a significant error in the current di/dt measurements. Therefore, a more accurate way to measure the current at which an inductor saturates is to measure the voltage across a small shunt resistor in series with the inductor.

Magnetics Design

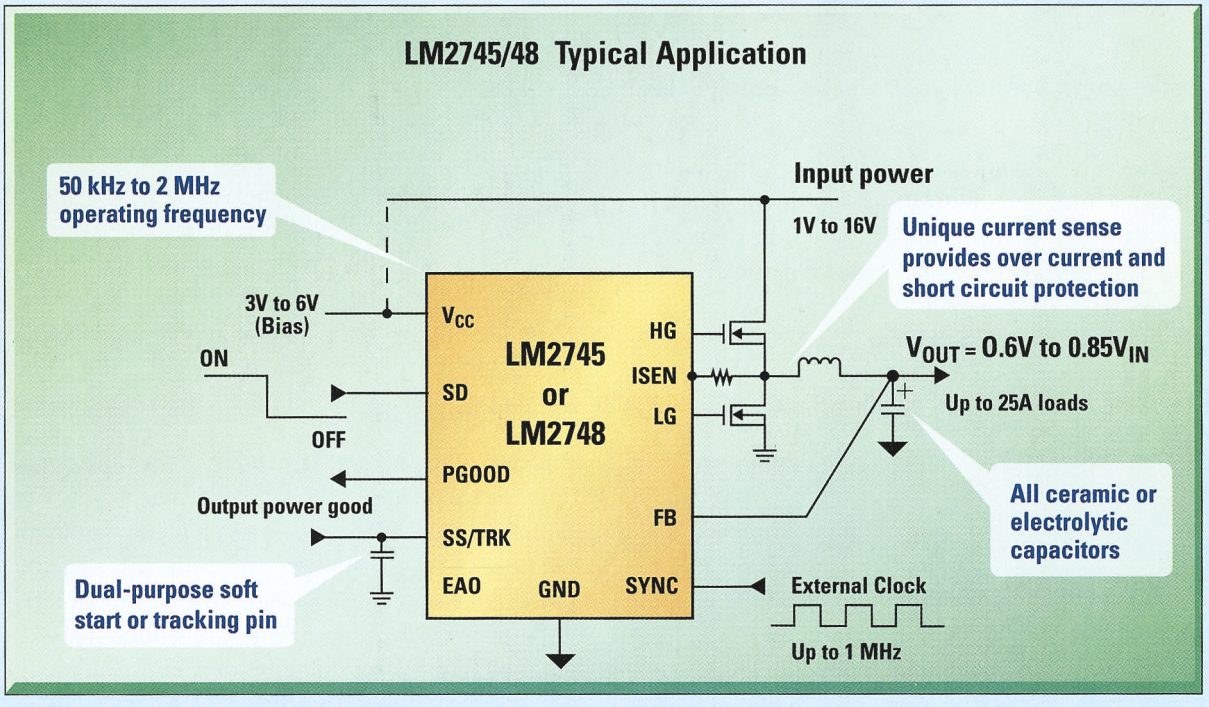
Another often overlooked issue is that of the reliability of the magnetic cores. Powdered iron is used as the core material in most output inductors because it is the lowest cost material available. Powdered iron cores are made from approximately 95% pure iron particles that are bound together with organic binders. The binders also insulate the iron particles from each other and provide a distributed air gap in the cores.

The powdered iron raw material used to form the cores contains small traces of impurities such as manganese (Mn) and chromium (Cr). The degree to which these impurities are controlled affects the reliability of the core. Examining the cross-section of the core using Spectral Electron Microscope (SEM) one can examine the relative distribution of impurities. Predictability of material and its supply chain are critical factors for core reliability.

Powdered iron cores are susceptible to a permanent increase in core loss when they are exposed to elevated temperatures for prolonged periods of time. This is due to the organic binders breaking down and resulting in an increase in the eddy current losses. This condition is referred to as thermal aging and can eventually result in thermal runaway of the core.

Industry's Only Controller with Pre-Bias Startup and Optional Clock Synchronization and Tracking

LM2745/48 Optimizes Design of FPGA, ASIC, and Point-of-Load Applications



LM2745/48 Features

- Input power from 1V to 14V
- Output voltage adjustable down to 0.6V
- Switching frequency from 50 kHz to 1 MHz
- Switching frequency synchronize range 250 kHz to 1 MHz (LM2745 only) Startup with a pre-biased load prevents sagging of output
- Power Good flag and output enable for easy sequencing output over-voltage and under-voltage detection ±1.5% feedback voltage accuracy over temperature
- Low-side adjustable current sensing
- Adjustable soft-start
- Tracking and sequencing with shutdown and soft start pins
- Available in a TSSOP-14 package

Ideal for achieving high efficiency and power density in 200W to 500W DC-DC converters

Product Highlight:

Flexible features for low voltage, high current power modules

Analyzing Power Modules

Factors that affect the core losses are the AC flux density, the operating frequency, the volume of the core, and the material type. At high frequencies, eddy current losses are the dominant loss mechanism, whereas at low frequency hysteresis losses dominate.

Eddy current losses, which result in heating of the core and reduced efficiency, are due to the existence of circulating currents within the body of a ferromagnetic material under conditions of time varying magnetic flux. Eddy current losses can be reduced by constructing the magnetic core with thin laminates of ferromagnetic materials rather than a solid piece. An example of such a core is Metglas, which are tape wound cores. Other magnetic vendors such as Magnetics Inc also produce tape wound cores.

To help magnetics designers core vendors like Micrometals (**www.micrometals.com**) provide the latest thermal aging information and calculations for their cores. Powdered iron cores that use inorganic binders that do not exhibit thermal aging are now available (such as 200C series cores from Micrometal)

Shoot-Through in Synchronous Buck Converters

Synchronous buck converters *(Figure 3)* are widely used in POL and PUPs supplies. A synchronous buck converter consists of a high side and a low-side MOSFET, which is placed in place of the conventional buck converter catch diode to provide a lower loss path for the load current.

One issue that is often overlooked in buck converter design is "shoot-through." Shoot-through is a condition in which both high-side and low-side MOSFETs are simultaneously fully or partially turned on, providing a current path from the input voltage to ground.

Shoot-through leads to current spikes at the switching instants and manifests itself as a decrease in the efficiency of the converter. A current probe cannot be used to measure it because the inductance of the probe significantly affects the circuit operation. An alternative way to detect shoot through is by looking for spikes on the gate source voltages of the two FETs. (The gate-source voltage of the top MOSFET can be monitored differentially).

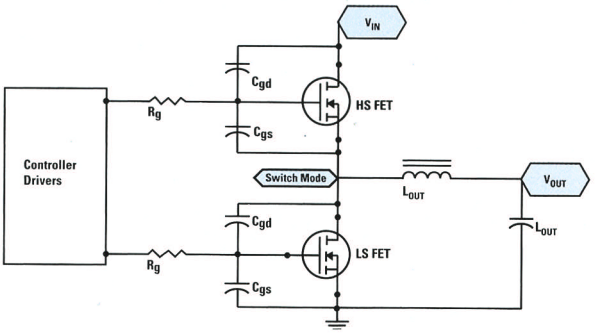


Figure 3. Synchronous Buck Converter

A number of techniques are used to minimize shoot-through.

One approach is to employ a controller IC with a "fixed dead-time," which ensures that there is a delay after the top MOSFET is turned-off before the lower MOSFET is turned on. This approach is simple, but has to be implemented carefully. If the dead time is too short, shoot-through may not be averted. If it is too long, the conduction losses increase because during the dead time the body diode of the bottom FET is on. Because of the conduction of this body diode during the dead-time, the efficiency of the system when using this technique depends somewhat on the bottom MOSFET's body diode characteristics.

Another approach is to use a controller IC with an "adaptive dead-time." In this approach, the gate-source voltage of the top MOSFET is monitored in order to determine when to turn-on the bottom MOSFET.

When the high-side MOSFET turns on, this induces dv/dt spikes on the gate of the low side MOSFET causing its gate voltage to rise *(Figure 4)*. If the gate-source voltage becomes high enough to turn it on, this will result in a shoot-through spike.

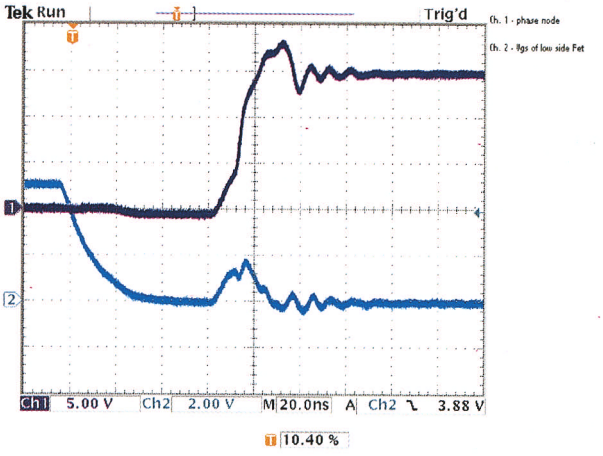


Figure 4. dv/dt induced step on the low-side MOSFET
Ch 1 Switch node
Ch 2 Vgs _ low-side MOSFET

Highly Efficient Intermediate Bus Converter

LM5033 Integrates Start-Up Regulator and Precision Reference

LM5033 Features

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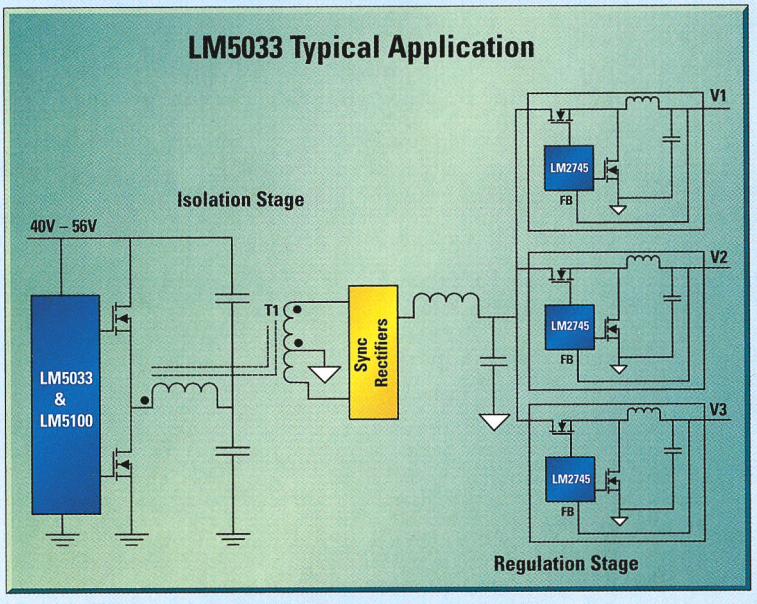
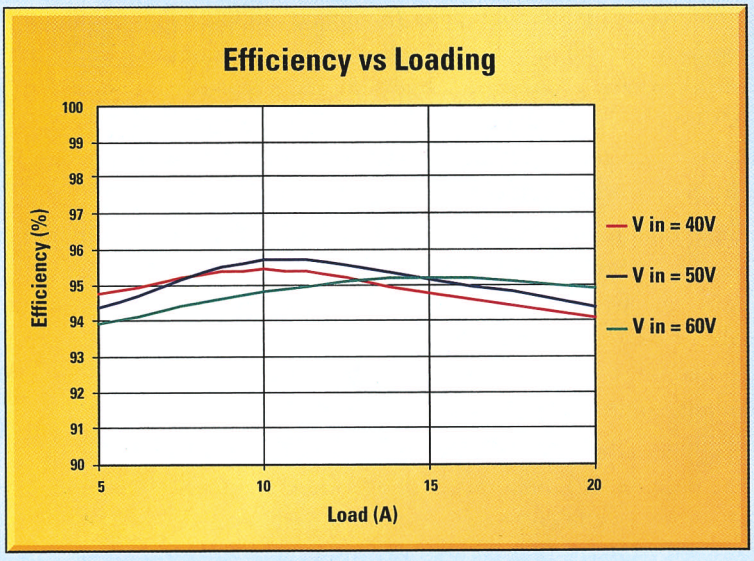
- No feedback opto-coupler required
- Integrated 15V to 100V start-up regulator
- Low primary component count
- Integrated 1.5A drivers
- Tiny, thermally enhanced LLP® packaging

Ideal for use in telecommunication bricks, industrial power converters, and automotive systems

Product Highlight:

Integrated start-up regulator, direct opto-coupler interface simplifies design of bus converters





Analyzing Power Modules

Adaptive dead time controllers monitor the MOSFET gate voltage externally. Thus, any added external gate resistors form a voltage divider with the internal pull down resistor of the controller. The gate voltage will actually be higher than the voltage monitored by the controller.

Predictive gate drive is an alternate approach where digital feedback is used to detect body diode conduction and to adjust the dead time delay to minimize the body diode's conduction, thus maximizing the efficiency of the system. This technique needs additional pins on the controller IC, increasing cost of the IC and the power module.

Note that predictive gate drive does not ensure protection against dv/dt induced turn-on of the FETs.

One way to minimize shoot-through is to slow down the turn-on of high-side MOSFET. This will reduce or eliminate the shoot-through, but at the expense of higher switching losses and lower efficiency. Proper selection of MOSFETs can also help to reduce the dv/dt induced voltage step on the gate of the lower MOSFET. A higher ratio of Cgs to Cgd will result in a lower voltage being induced on the gate of this MOSFET.

Test conditions for shoot-through are often overlooked during load transients especially when the load is released, or reduced suddenly, which results in the controller producing narrow pulses. Most of today's high-current applications utilize multiphase designs using driver ICs to drive the MOSFETs. Driver ICs add another dimension to the shoot-through issue, especially during transient conditions. The presence of narrow drive pulses, in conjunction with propagation delays in the driver, can result in shoot-through.

Most driver IC manufacturers are adding minimum pulse-width requirements, i.e. if the pulse from the controller is below a minimum pulse width, no pulse is applied to the gate of the MOSFETs.

Another feature that is designed in by IC manufacturers is programmable dead time *(T_{RT})*. This is enhancement to adaptive transition timing. A resistor from the RT pin (deadtime programmable pin) to ground programs dead time between high and low side transitions. This, in conjunction with propogation delay (tp), disables the complementary MOSFET during transitions, and prevents shoot-through in synchronous buck converters.

Reliability

Thorough testing of a module at an early stage is critical to ensure a reliable design and obviate last-minute surprises. Testing the module in the customer's system is critical to ensure that all possible factors that can cause failure such as fan failure, partial blockage of fans etc, have been considered. Distributed architectures demand that the system be in service for many years with little or no downtime. Since the calculated MTBFs of power modules are in the several million hour range, this goal is not hard to achieve.

However, one thing that is often overlooked is the reliability of the PCB. With the trend in present designs of processing ever higher currents on ever smaller PCBs, the increased current density can cause buried and other vias to malfunction.

It is critical that buried vias on the PCB that have to carry significant current have adequate copper surrounding them to provide the design robustness. This also minimizes z-axis thermal expansion, which can result in open vias when the PCB is subjected to temperature variations during manufacturing as well as during its product application. PCB design must be reviewed thoroughly with feedback from PCB manufacturers. Thus PCB manufacturers can provide feedback with regards to robustness of PCB design based on their manufacturing capabilities.

Summary

To implement a reliable power supply system using modules, a number of issues relating to design robustness must be addressed. Issues highlighted in this article include: reliability of powdered iron magnetic cores, magetics, shoot-through in synchronous buck converters, and reliability of the PCB in high-current applications. ■

Acknowledgement: Author thanks Mr. Tushar Dhayagude and Dr. Haachitaba Mweene for their feedback on the article.

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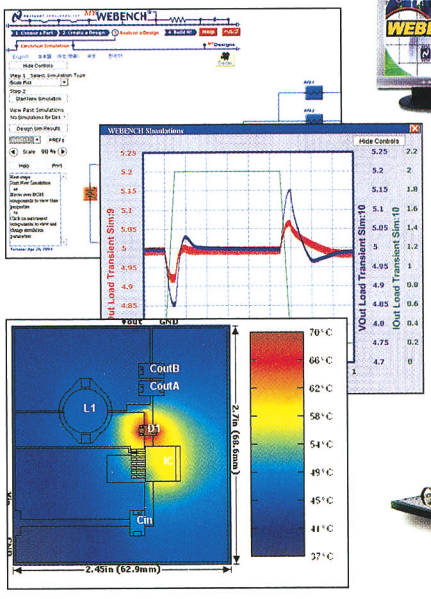
Power Design Tools



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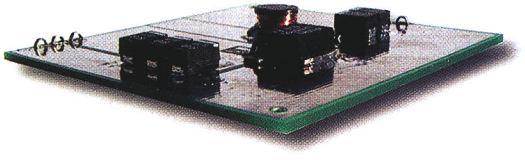

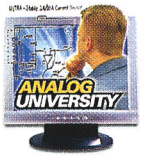

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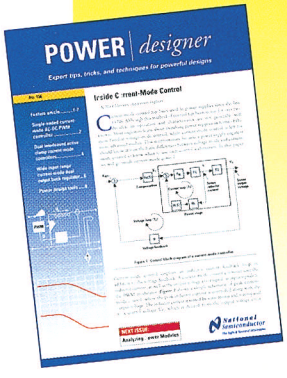

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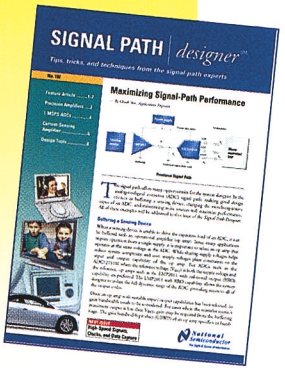

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THE 32ND ANNUAL MICROPROCESSOR DIRECTORY

BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Charting your course

FOLLOW THE SILICON-BREAD-CRUMB TRAIL IN THIS DIRECTORY TO FIND THE PERFECT DEVICE FOR YOUR PROJECT.

Welcome to the 32nd *EDN* Microprocessor/Microcontroller Directory. The number of companies and devices the directory lists continues to grow, and, once again, we've expanded the company roster and table of devices by at least 10%. This continuing growth is a testament not only to the variety of processors available, but also to the tremendous variation among requirements, features, and the increasing range of applications for which designers are using microcontrollers.

Is this growth in processor options a precursor to an industrywide consolidation? Not likely. Successful microcontroller offerings and embedded-system-application designers stress the optimum balance of processing performance, power consumption, and bill-of-materials costs, which vary so significantly across the growing range of embedded-system applications that few microcontroller-product families are in direct competition. Some of the companies participating in this year's directory have for years been selling processor product lines but only recently began making them available to the engineering public.

This directory aims to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. This print version offers an abridged, high-level overview of this year's participating companies and their products; the online version is complete. The device tables, due to their size, are available exclusively at www.edn.com/050804cs as a set of PDF files that you can view or print across two pages. The tables list only software-programmable processors, including cores and programmable-logic devices with embedded cores. The directory does not include DSPs; *EDN* lists DSPs in its annual DSP Directory, which it publishes six months out of phase with this one.

We welcome your feedback, because it can help us to make next year's directory more useful to you. Send your feedback to mpdirectory@edn.com. As always, if this directory helps you choose a processor, please let the vendor know how you found its part. And if you cannot find your favorite processor company or device, please let both the company and *EDN* know that you missed reading about it in the directory.

ACTEL CORP

Actel offers processor cores as part of its DirectCore product offerings, which range from the 8-bit 8051 to the 32-bit ARM7. The company sources, verifies, and supports these IP (intellectual-property) processor cores and maintains them as pre-implemented, synthesizable building blocks for use with Actel FPGA devices. Actel and ARM collaborated to develop and offer an ARM7 family microprocessor for use with Actel's FPGA devices to support applications ranging from high-volume-consumer to high-performance, high-reliability products. Actel will deliver the "soft" ARM7 family core with a license-free business model.

Designers can use the Core8051 8-bit microcontroller core in Actel's nonvolatile, single-chip FPGAs, including ProASIC3, ProASIC Plus, Axcelerator, SX-A, and RTSX-S. The Core8051 executes all ASM51 instructions—most in one clock cycle.

Designers can combine the Core8051, available in RTL (VHDL or Verilog) or netlist form, with other Actel DirectCore IP products. Actel's Platform8051 development kit includes a development board, IP cores, software, and FPGA tools that enable designers to design, configure, and program Core8051 designs into Actel FPGAs.

ADVANCED MICRO DEVICES

AMD (Advanced Micro Devices) continues to broaden its x86 and Alchemy product offerings. Its x86-based product line spans the embedded-system market, targeting enterprise-class servers and workstations, and it extends the x86 ISA (instruction-set architecture) across 32- and 64-bit PC, server, and workstation platforms with the AMD64 technology. Subsequent enhancements of the AMD Athlon and AMD Opteron processor lines extend 64-bit x86 computing to the embedded-system market. The ÉlanSC5220 x86 controller covers the data-communications, telecommunications, and information-appliance markets. AMD devices also target PDAs, Web tablets, portable and wired Internet-access devices, and gateway applications with MIPS-based Alchemy microprocessor offerings.

The AMD Geode processor family delivers optimized x86 performance with reduced power consumption targeting broadband multimedia, set-top boxes, tablet PCs, HDTVs, kiosks, network appliances, and thin-client applications. Each Geode processor uses a nomenclature that identifies a performance-power rating to assist designers in selecting a processor with the optimum mix of power and performance. For example, the recently introduced AMD Geode LX 800@0.9W processor can run a full-featured Windows or Linux operating-system application at less than 1W in a fanless environment. AMD added the Alchemy Au1200 processor to the AMD Alchemy line to better target low-power, high-performance PMP (personal-media-player), automotive, and DMA (digital-media-adapter) applications.

ALTERA

Altera continues to improve its integrated-product portfolio. HardCopy II uses a fine-grained collection of Hcell transistors. It builds on the company's line of structured-ASIC offerings and supports seamless migration from FPGA to ASIC implementations and provides the density, cost, performance, and power benefits of ASIC technology. Altera's Stratix II EP2S180 device, its largest and fastest FPGA, uses a new logic structure that enables a faster memory-core frequency. The new EPM-2210 device is the largest member of the Max II family of low-cost, high-density, and high-performance CPLDs.

The Nios II family of embedded processors features a general-purpose RISC CPU architecture to address a range of embedded-system applications. The Nios II family comprises three cores—fast (Nios II/f), economy (Nios II/e), and standard (Nios II/s)—each targeting a specific price and performance range. The Nios II processor works with all the latest Altera FPGA families. Developers can use a Nios II processor to augment an external processor by offloading tasks to maintain overall system performance.

ANALOG DEVICES

Analog Devices offers high-performance semiconductors for signal-processing. The 16/32-bit embedded Blackfin processor targets the computational demands and power constraints of embedded audio-, video-, and communications-system applications. Blackfin uses a 32-bit RISC microcontroller-unit programming model based on an SIMD (single-instruction-multiple-data) architecture to deliver signal-processing performance and power efficiency. In January 2005, Analog introduced the network-enabled ADSP-BF534, BF536, and BF537 processors, as well as the BF566-eM30 eMedia Platform, which targets IP set-top boxes, triple-play devices, portable and networked media players, and automotive-safety/driver-assistance systems.

The ADuC702x precision analog-microcontroller family combines on a single chip embedded precision analog functions and digital programming. Featuring ARM7-based programmability, the ADuC702x is the newest addition to the company's MicroConverter series—a portfolio of 8052-based devices. MicroConverter products target high-precision measurement and control and data-acquisition systems with basic digital-programming needs. The precision analog microcontrollers integrate a 32-bit RISC core and flash memory with precision data-conversion technology that supports as many as 16 channels of fast, 12-bit-accurate analog-to-digital conversion and as many as four 12-bit DACs.

APPLIED MICRO CIRCUITS CORP

Since acquiring a portfolio of products associated with IBM's 400 PowerPC processors less than a year ago, AMCC (Applied Micro Circuits Corp) has introduced new processors to its portfolio of ASSP (application-specific standard products). The PowerPC 440SPe targets RAID (redundant-array-of-independent-disks) controllers and SAN (storage-area-networking) equipment by supporting three independent PCI Express interfaces and one PCI-X Version 2.0 interface. The 440GR processor targets low-power applications, such as line-card system control and multiradio devices. The 440EPx and 440GRx include an optional integrated security accelerator or Turbo Security Engine that provides IPsec (Internet Protocol security) and SSL (Secure Sockets Layer) acceleration supporting bandwidth of more than 500 Mbps. AMCC's Turbo Security Engine secures communications protocols over wired or wireless networks, supports VPNs (virtual private networks), and provides secure Internet-based transaction processing.

AMCC's 400-series portfolio, which it built on the PowerPC architecture, comprises the S-, G-, and E-series product categories. I/O-centric S-series products feature PCI Express and PCI-X interfaces targeting storage and networking applications. S-Series devices support DDR667 SDRAM and RAID XOR. Gigabit Ethernet-centric G-Series devices offer high integration and support for DRAM, PCI, and optional security; they target applications requiring control-plane processors. E-Series products target imaging, wireless-access, and industrial-control applications; they support low-cost embedded-system control and include FPUs, Ethernet, USB, PCI, and DDR SDRAM.

ARC INTERNATIONAL

ARC International offers two families of 32-bit processor cores. ARC 600 cores target battery-operated and cost-sensitive products in the embedded control-, consumer-, networking-, and automotive-system markets. ARC 700 cores deliver the computing power for graphics, media, and packet

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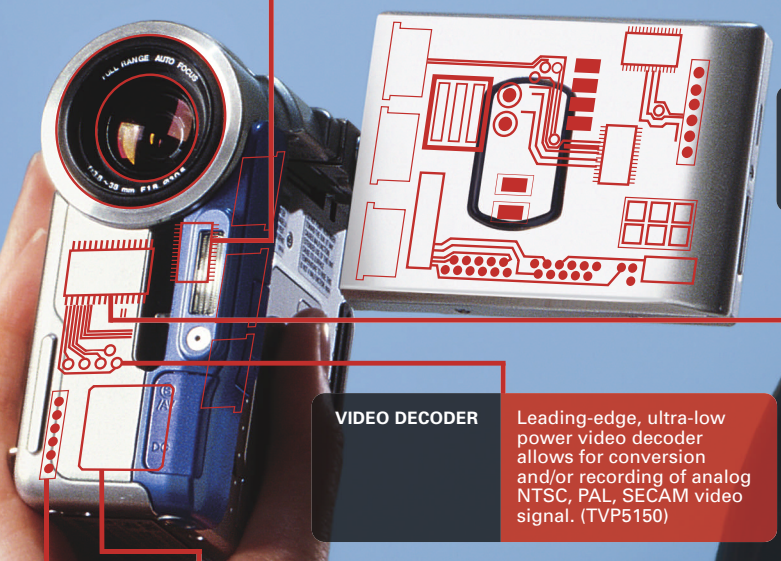
POWER MANAGEMENT
Battery management with integrated charging FETs and synchronous DC/DC power conversion simplifies design and maximizes battery life. (TPS65010)

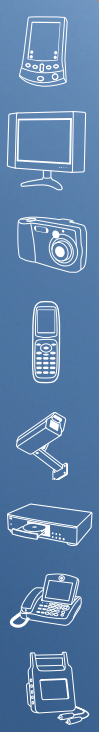


AMPLIFIER
High-speed video amp seamlessly interfaces with DACs embedded in video processors. (OPA360)

VIDEO DECODER
Leading-edge, ultra-low power video decoder allows for conversion and/or recording of analog NTSC, PAL, SECAM video signal. (TVP5150)

DSP
TI's DSP-based digital media processors come with razor-sharp reflexes, making them easily programmable to adapt to new standards:
- Imaging: JPEG, MJPEG, JPEG2000
- Video: MPEG-2, MPEG-4, H.26x, Microsoft® WMV9
- Audio: MP3, AAC, Microsoft WMA9, G.7xx
- Media Transmission: RTP, TCP/IP, 802.11

INTERFACE
TI's 1394 and USB ICs enable streaming A/V and file transfer over high-performance digital links. (TUSB6250)



Jump-start your design with TI's solutions for your entire signal chain. From industry-leading DSP-based digital media processors and high-performance analog to logic and an extended portfolio of application software, TI delivers reliable, scalable and power-efficient video and imaging solutions. With TI, you can fast-forward your product to market.

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processing; they also target high-end embedded-system platforms using OSs such as Linux.

ARC's configurable processor technology enables SOC (system-on-chip) designers to optimize a processor core for their applications, in die area, power, and performance of critical code. Designers can remove core features by using the ARChitect configurator tool's drag-and-drop GUI. Configurable items include caches, interrupts, DSP options, timers, debugging components, type and size of core registers, bus widths, and instruction-set options.

Using ARChitect's extension wizard, designers can add custom instructions, registers, and logic to reduce the number of cycles that critical code requires.

▶ARM

ARM licenses IP (Intellectual property) for the development of 32-bit RISC-microprocessor-based SOCs (systems on chips), and ARM-powered microprocessors target automotive, consumer-entertainment, imaging, networking, storage, security, and wireless applications. ARM offers a range of processor cores, including the ARM7, ARM9, ARM10, ARM11, ARM Cortex-M3 processor, and MPCore multiprocessor families. ARM offers the SecurCore technology targeting secure applications, such as smart cards and SIMs (subscriber-identity modules), and the OptimoDE Data Engine signal-processing technology and MBX 2-D- and 3-D-graphics-accelerator cores, which it developed with Imagination Technologies. ARM offers supporting software, such as TrustZone technology for data security, Jazelle Java acceleration software, Swerve 3D, and Intelligent Energy Manager.

The ARM Cortex processor family offers high performance at the lowest cost and power consumption; all Cortex cores implement the Thumb-2 instruction set to address the increasing performance and cost demands of various markets. The ARM Cortex family of processors consists of the A, R, and M intelligent computer architectures. The ARM Cortex-A series targets demanding consumer-entertainment and wireless products running complex operating systems and implementing sophisticated user interfaces. The ARM Cortex-R series focuses on the application needs of real-time systems. ARM Cortex-M devices provide the benefits of 32-bit development to the microcontroller market. The ARM Cortex-M3 processor, the first core available from the ARM Cortex family, targets the requirements for high system performance in extremely cost-sensitive embedded-system applications, such as microcontrollers, automotive-body systems, white goods, and networking devices.

▶ATMEL

Atmel offers six flash-based microprocessor architectures: the 4-bit automotive and RF Marc 4; the high-performance, low-power 8/16-bit RISC AVR; the AT89 single-cycle CISC 8051; the 32-bit ARM7, ARM9, and ARM11 microcontrollers; and the PowerPC and SPARC architectures. Flash densities for Atmel microcontrollers reach 256 kbytes; SRAM reaches 32 kbytes. Packages offer pin counts of eight to 256 pins. Ultralow-power devices are available with as little as 100 nA of standby power. ROMless, ROM, and OTP (one-time-programmable) devices are available for volume production.

Atmel develops platform ASICs and ASSPs (application-specific standard products) based on its microprocessor families. Its 8051-based ASSPs include CANs (controller-area networks), MP3, smart-card readers, USB host/client, and Web-embedded TCP/IP. AVR-based ASSPs include the Z-link ZigBee-specific baseband controller and the TPM (Trusted Platform Module), which provides hardware-based security for laptops, PCs, and network servers.

New offerings include the AT89LP single-cycle, 20-MIPS 8051, which drops into MCS-51 sockets and targets increasing performance requirements in legacy 8051 products, principally in the Asian market. The FPSLIC (field-programmable system-level IC) II is a 20-MIPS AVR RISC processor, integrated with a dynamically reconfigurable FPGA fabric and supported by design tools that allow multiple interfaces, operators, or peripherals to share the same silicon at different times during runtime. FPSLIC II's dynamic, runtime reconfigurability allows it to execute more functions at a lower silicon cost and with less power consumption than a conventional FPGA.

The 32-bit, ARM7-based AT91SAM7 family targets 8- and 16-bit designs that need 32-bit performance, more memory, and supervisory functions, but its price is comparable with 8/16-bit devices and development tools. The AT91SAM7 provides features for real-time 8- and 16-bit designs, including power on reset, brownout detection, watchdog timer, RC oscillator, and bit-manipulation capabilities.

▶BROADCOM

Broadcom provides a family of high-performance, low-power, integrated SOC (system-on-chip) processors targeting data-networking and communications applications, as well as security, storage, 3G wireless infrastructures, and high-density computing. The new Broadcom broadband processors integrate as many as four 64-bit MIPS processor cores onto a single die. This configuration achieves higher aggregate performance than multiple discrete cores and dramatically reduces board space and power dissipation.

CMP (chip multiprocessing), an advanced technique in CPU design, integrates two or more processor cores into one chip to enhance computing performance. CMP scales system performance by sharing the workload across multiple cores and relies on high-speed, on-chip interconnects and high-bandwidth pipes to memory and I/O. A benefit of CMP is power efficiency, especially because the classic technique of scaling performance by increasing core frequency has reached the point of diminishing returns. Power and leakage are formidable challenges as designs become more complex with increasing numbers of transistors on one die.

Broadcom manufactures its family of dual- and quad-core processors based on the BCM1250's multicore architecture. The memory-controller design addresses bandwidth and efficient channel usage. The controller supports DDR-400 and DDR2-800 for a peak bandwidth of 100 Gbps, supporting higher data-plane-forwarding performance. Configurable as two 64-bit-wide channels or four 32-bit-wide channels for improved memory usage, the memory controller supports as much as 16 Gbytes of memory with 1-Gbit DRAM technology.

▶CAMBRIDGE CONSULTANTS

Cambridge Consultants, a 250-person, multidisciplinary organization, provides product-design services for high-precision analog, mixed-signal, and RF on CMOS. It also offers software and silicon IP (intellectual property) for its 16- and 32-bit XAP processor cores and the APE datapath signal-processing engine. The 16-bit-Harvard-architecture XAP1 and XAP2 cores target projects requiring low power and low gate count. XAP1 is a 3000-gate core featuring an 18-bit instruction word for programs running from on-chip ROM. The 12,000-gate XAP2 supports both 16-bit program and data memories as large as 64k words.

Cambridge Consultants recently announced the XAP3 ASIC processor core, a 32-bit soft RISC core featuring high code density with options for synthesis to ASIC or FPGA devices. The XAP3a is a 40,000- to 50,000-gate, two-stage pipeline Von Neumann processor with a new ISA (instruction-set architecture) that delivers high code density and operating-system support.

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LM95231 - Precision Dual Remote Diode Temperature Sensor (RDTS) with TruTherm Technology

TruTherm Technology

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- Reduces chances for device overheating, enables precise fan control which lowers acoustic noise

LM95231 Key Features

- Two remote and one local sensor
- Analog and digital filters to reduce noise
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- Remote diode fault detection
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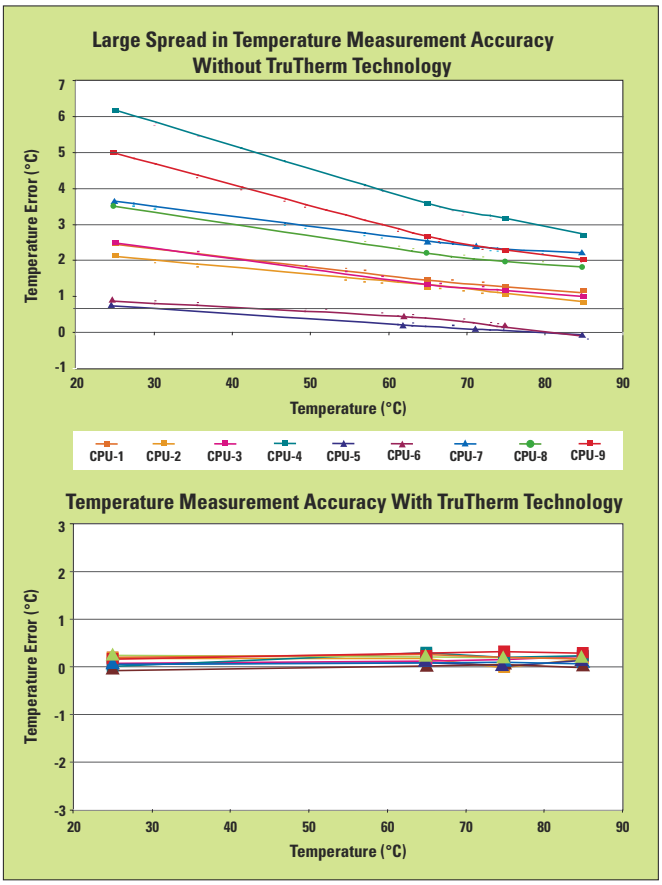

Key Specification (Typical)	
Remote Diode Temperature Accuracy	
TA=30°C to 50°C, TD=45°C to 85°C	±0.75 °C (max)
TA=0°C to 85°C, TD=25°C to 140°C	±2.0 °C (max)
Local Temperature Accuracy	
TA=0°C to 85°C	±3.0 °C (max)

Supply voltage: 3.0V to 3.6V, Supply current: 2 mA (typ.)

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▶CAVIUM NETWORKS

Cavium Networks offers silicon for security, network-services, and embedded-processing applications. Cavium Networks' Nitrox and MIPS64-based Octeon families of processors and accelerator boards offer flexible, scalable, and highly integrated platforms delivering 50-Mbps to 10-Gbps performance. The company's products target networking equipment that includes routers, gateways, network appliances, wireless-LAN access/aggregation points, and storage-networking devices.

The Octeon multicore MIPS64 processors address the needs of networking equipment ranging in performance from 200 Mbps to 10 Gbps. The Octeon family offers a scalable, software-compatible processor line with two to 16 MIPS64-based cores in one chip and power ranging from less than 5 to 29W. Octeon devices include hardware acceleration essential for Level 3 to Level 7 applications, which includes packet processing, TCP, multicore scaling, compression/decompression, pattern matching, and encryption.

The Nitrox Soho Secure Communication Processor family targets wired and wireless broadband gateway for the SOHO (small-office/home-office), and SME markets, with performance requirements ranging from 10 to 200 Mbps. The highly integrated, MIPS-32-based Nitrox SOHO-processor SOC (system-on-chip) products include IPsec (Internet Protocol security) and SSL (Secure Sockets Layer) acceleration.

▶CIRRUS LOGIC

Cirrus Logic's EP93xx ARM9-based embedded processors target applications such as point-of-sale terminals, medical instrumentation, security and surveillance, process monitoring, and digital entertainment. These processors include WinCE.NET board-support packages and Linux kernel ports with Cirrus Logic's ARM third-party program support.

MaverickKey technology, which is standard on all Cirrus ARM9-based embedded processors except the EP9301, comprises the MaverickKey digital-rights-management tool and the MaverickCrunch advanced, mixed-mode, math coprocessor. MaverickKey technology allows designers to assign hardware IDs to protect against design piracy as products enter manufacturing. The MaverickCrunch engine greatly accelerates the single- and double-precision integer and floating-point processing capabilities of the ARM920T processor core.

▶CRADLE TECHNOLOGIES

Cradle's new MDSP (multiprocessor-DSP) family, the CT3600, comprises three members. The CT3600 family provides flexibility for designers to choose a device that best fits their media-processing application. With as much as twice the computational elements and 1.5 times the operating frequency of the CT3400, the CT3600 family leverages the same MDSP architecture its predecessor uses and scales the performance and throughput by as much as four times. Power consumption is 1 to 5W, depending on device size, application, and operating frequency.

The CT3600 family extends the performance and scalability of the CT3400. The new family comprises two computational Quads, adding memory and processing power to the architecture. Cirrus removed the I/O Quad as a separate block, instead dividing the I/O-pin groups into two sets, each being associated with a compute Quad.

The CT3600 product family integrates as many as 16 loosely coupled SIMD (single-instruction multiple-data), 32-bit DSP engines; eight general-purpose CPUs; 144 programmable I/O pins; and a three-tiered memory hierarchy system to accelerate and integrate multimedia infrastructure processing.

The CT3400, with eight DSP cores and six general-purpose processors, runs at 230 MHz and can deliver more than 29,000 MMACS. Each DSP core has its own local instruction memory and data-register file (128 32-bit registers), allowing the cores to operate mostly autonomously. The compute Quad provides 64 kbytes of shared data memory and 32 kbytes of instruction cache, used by the four general-purpose processors.

▶CYAN TECHNOLOGY

Cyan Technology's low-power, 16-bit, embedded-communications, flash-based eCOG1k microcontroller implements a 25-MHz RISC Harvard architecture that includes internal flash memory, RAM, and cache. The external-memory interface supports addressability of 32 Mbytes of external memory. Additional features include a Smart Card interface, a 12-bit A/D converter; a temperature sensor; and a proprietary-port configurator. Cyan's CyanIDE development software includes a full ANSI unlimited-C compiler, simulator, debugger, and peripheral-configuration software. Users can select those peripherals they need and connect them to a choice of pins. The peripheral-register setup code is automatically generated in assembly language. All Cyan development software is downloadable and free.

▶CYBERNETIC MICRO SYSTEMS

Cybernetic Micro Systems produces a line of ASICs to interface to a variety of peripherals that would be difficult to control from a general-purpose computer. These chips provide a programmable interface to the low-level functions of the peripheral. The 100-pin, 8-bit P-51 microcontroller either sits between the host computer and the peripheral device or becomes the peripheral device. With a dual-port RAM interface on the host side (PC104/ISA format), the P-51 looks like memory to the host but has the intelligence and capability of an 8051, including a special square-root function, for the peripheral application.

▶CYPRESS MICROSYSTEMS

Cypress MicroSystems' field-programmable, mixed-signal PSOC (programmable-system-on-chip) arrays target embedded-control functions in consumer, industrial, office-automation, telecom, and automotive applications. PSOC devices integrate an 8-bit processor core with programmable blocks of analog and digital logic in eight- to 100-pin devices in DIP, SSOP SOIC, MLF, and TQFP packages. All PSOC devices are dynamically reconfigurable during runtime, enabling designers to create system functions that can achieve more than 120% usage of the die.

The new CY8C24x94 family adds full-speed USB to the conventional PSOC features to create an economical full-speed USB microprocessor. It targets consumer electronics, HIDs (human-interface devices), and home and industrial automation. The CY8C21x23 and CY8C21x34 families are Cypress' smallest and least costly PSOCs with four digital and four analog configurable peripheral blocks. The general-purpose CY8C21x34 microcontroller supports capacitive touch-sense applications with no external components. These PSOC families target consumer and industrial-control applications, such as CapSense; fan controllers; battery chargers; security sensors and control; large sensor arrays; and smart temperature, pressure, and flow sensors.

The CYWUSB6953 PROC (programmable radio on chip) incorporates a PSOC device and wireless-USB technology in one integrated device. In addition to standard PSOC resources, the PROC includes a DSSS (direct-sequence spread-spectrum), 2.4-GHz radio system.

The CY8C42xxx family features a new high-voltage PSOC that can operate at a drain-to-drain voltage of 2.5 to 36V. In addition to the standard PSOC resources, it adds linear and switching control loops and high-voltage I/O, improves analog absolute accuracy, and is available with and without integrated FETs. The high-voltage PSOC targets power supplies, battery chargers, and white-LED drivers.

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DALLAS SEMICONDUCTOR MAXIM INTEGRATED PRODUCTS

Dallas Semiconductor offers four families of 8051-instruction-set-compatible microcontrollers that combine internal and I/O options with proprietary core designs to provide high-performance 8051 derivatives. Devices include one-clock/machine-cycle parts that can achieve operating speeds approaching 33 MIPS. The memory configurations for these devices are ROMless, EPROM, and in-system-programmable flash memory ranging to 64 kbytes. The secure microcontrollers target applications demanding protective measures against IP (intellectual-property) theft. These devices employ encryption techniques that support ATMs, point-of-sale terminals, and data-logging applications.

The network microcontrollers provide low-cost connections for networking applications and include a built-in Ethernet MAC (media-access controller), complete TCP/IP-address stacking in ROM, CAN (controller-area networking), and parallel and serial ports. The devices use a microcontroller core running at 75 MHz with an extended 22-bit addressing range. The mixed-signal microcontrollers feature 12-bit analog-to-digital conversion and dual 8-bit PWM channels that are combinable to 16 bits, as well as multiple serial ports and extended parallel I/O.

EM MICROELECTRONIC

EM Microelectronic's microcontrollers target applications that need ultralow current consumption, such as toothbrushes, shavers, scales, radio-controlled clocks, toys, headphones, TMPS (temperature-monitor power supply), metering, heat cost allocation, HVAC, smoke detectors, insulin pumps, security, sports, computer peripherals, and termination lines in communication. Product offerings include ROM or flash memory; as many as four multiplexer LCD drivers; an RC oscillator, a crystal oscillator, or both; EEPROM; an ADC; and high-drive outputs.

During the previous year, EM Microelectronic introduced the 8-bit, CoolRISC-based EM6812 family of microcontrollers, which targets industrial, consumer, computer peripherals, and automotive applications. The EM6812 consumes 0.15 mA in sleep mode, 0.8 mA in standby mode, and 120 mA in active mode; it operates at 2 to 5.5V. It has a function for fast wakeup from standby mode and operates at as much as 10 MHz (RC) or on a 32-kHz crystal oscillator. Additional features include a single-slope ADC, on-chip brownout detection, power-check functions at start-up, and flash read monitor.

FREESCALE SEMICONDUCTOR

The 32-bit ColdFire processor family targets markets that require control, connectivity, and security in an integrated device. Building on its 68K legacy, Freescale expanded the ColdFire-processor family to meet the needs of the low-end, 32-bit-system market. The two new 32-bit families, MCF520x and MCF521x, enable designers to reduce memory, power dissipation, system-board size, and system costs.

Freescale's 32-bit PowerQuicc line consists of integrated communications processors based on the PowerPC core that provide data- and control-plane processing for wireless and wire-line infrastructure, enterprise networking, home and SOHO (small-office/home-office) networking, and pervasive computing.

Freescale's high-performance PowerPC processors with AltiVec technology also support these applications. Freescale designed its new MPC8360E PowerQuicc II Pro communications processor family with Quicc Engine technology to reduce the cost of developing packet-based networking and wireless equipment. Freescale's latest PowerPC processors, including the MPC7447A and 90-nm MPC7448, deliver gigahertz-class performance at less than 10W.

The company introduced the MAC7100 family for designers who need 32-bit performance for cost-sensitive automotive-body, -chassis, and -safety applications. Freescale's 16-bit, single-chip, 10/100-Mbps MC9S12NE64 Ethernet device can replace multichip Ethernet offerings. Freescale introduced the single-core MPC5200-B telematics- and automotive-infotainment processor, boasting 885 MIPS and capable of handling audio compression decoding and encoding and video decoding.

FUJITSU MICROELECTRONICS AMERICA

Fujitsu's 32-, 16-, and 8-bit microcontrollers include general-purpose and application-specific versions, targeting automotive, communications, computer-peripheral, industrial, and consumer applications.

Fujitsu's premier FR60 Lite series provides 32-bit performance at 16-bit prices for mobile devices and consumer products, with versions that include LCD controllers and feature power requirements as low as 1 mA/MHz. The newest FR60 Lite versions, the MB91F267 and MB91266, incorporate multifunction timers for inverter control of motors in advanced air conditioners, refrigerators, washing machines, vacuum cleaners, and other appliances. Inverter equipment inputs a dc that the system changes into ac. The 32-bit RISC core in the FR60Lite series meets power requirements of less than 2 mA/MHz. The RISC core completes basic instructions in one clock cycle with an optimized pipeline.

Fujitsu's new family of microcontrollers, the MB9140x series, targets network-enabled household appliances. These 32-bit microcontrollers incorporate networking-security features, onboard ROM and RAM, and support for IPv6. The MB9140x supports IPv6 and includes encryption circuitry supporting the AES (Advanced Data Encryption Standard), DES (Data Encryption Standard), and 3DES (Triple DES). The encryption circuits are 150 to 200 times faster than software-based encryption and are complemented by authentication circuitry. The series also supports the MD5 (Message Digest 5) and SHA1 (Secure Hash Algorithm 1) authentication standards, key exchange methods DH 1/DH 2, and the IKE (Internet Key Exchange) protocol with a hardware engine.

The newest members of Fujitsu's 8-bit F2MC-8FX series, the MB95F118 and MB95F108H, integrate 60-kbyte dual-operation flash, a LIN (local-interconnect network), multiple PPGs (programmable pulse generators), and a 10-bit ADC. The instruction-cycle time is as fast as 100 nsec.

GOAL SEMICONDUCTOR

Goal Semiconductor offers a range of 8-bit microcontrollers targeting embedded data-acquisition systems. Its latest family of high-performance microcontrollers is 8051-compatible and operates at 40 MIPS. The VRS2000, the first family in this new series, includes an advanced hardware-arithmetic unit and flash programming, debugging, and emulation with a JTAG interface. The VRS2000 provides a one-chip platform for applications from industrial control and instrumentation to portable and medical devices.

Goal's other products include mixed-signal and low-cost industry-standard flash 8051 microcontrollers for embedded systems in industrial, consumer, instrumentation, automotive, and communication markets. The Versa Mix family of integrated, mixed-signal 8051 microcontrollers targets signal-conditioning, data-acquisition, processing, and control applications. Features for these devices include a hardware multiply-accumulate unit, an ADC, an op amp, a current source, digital potentiometers, and communication interfaces. The Versa microcontroller series of low-cost, 8-bit, 8051-based microcontrollers are cost-efficient drop-in replacements for industry-standard devices. The VRS1xxx family of Versa microcontrollers features ISP/IAP (in-system-programming/in-application-programming) capability.

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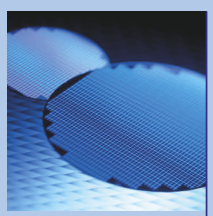

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[1]iSuppli, 2005 and Gartner Dataquest, 2004

Never stop thinking.

▶HYPERSTONE

The Hyperstone family of 32-bit single-core, RISC/DSP processors perform parallel RISC- and DSP-instruction execution. They achieve fast execution of RISC/DSP instructions with the use of an ALU for normal RISC-instruction execution, and a separate DSP-instruction execution unit. The devices execute RISC and DSP instructions transparently to the user and with a high degree of parallelism, sharing a set of registers. All instructions, including those performing DSP functions, use RISC principles based on the load/store architecture. Instructions are variable in length to be memory- and speed-efficient. The E1-32XSR/XSRU processor cores target low-cost, compact, and energy-efficient designs.

During the previous year, Hyperstone introduced the HyNet32S networking processor, a cost-effective version of the HyNet32XS that the company also bases on a core similar to the E1-32XSRU RISC/DSP processor core. It can operate at a maximum clock rate of 200 MHz and includes a YuV interface for CCIR656-compliant video input, as well as 10/100-Mbps Ethernet support. The HyNet32S employs four internal buses with a six-channel DMA controller to complement internal RAM, boot ROM, dual instruction/data caches, an MMU, and a time-processor unit.

▶INFINEON TECHNOLOGIES

Over the previous year, Infineon introduced its first 8-bit microcontroller with on-chip flash; six new 16-bit microcontrollers for automotive and industrial applications; and three TriCore-based microcontrollers, including the first with embedded flash. Infineon's processors are available as stand-alone devices and embedded-processor cores. The devices in the 8-bit C500 and C800 families are compatible in architecture and software with the 8051 microcontroller. The XC866 is a warp core-based device with on-chip flash, an ADC, and a motor-control unit that targets industrial-motor-control, automotive-body, and consumer drives.

The 16-bit C166 family of microcontrollers targets industrial-control, automotive-electronics, PC-peripheral-control, and consumer-electronics applications. The XC164CM provides double the performance at the same clock speed as earlier generations of the C166. The XC164N/D/S device families offer a scalable peripheral set, including a CAN (controller-area network), an ADC, and motor control for industrial applications. The XC167CI/CS/CS family of microcontrollers features large embedded flash memory to support applications such as electronic power steering. The XC164S/D/N peripherals include capture/compare, CAN controller, and MAC (multiply-accumulate) units for robotics, networked systems, and other industrial-control applications.

The TC1100/TC1115 TriCore microcontrollers target robotics and industrial-networking applications, as well as industrial high-performance electrical-motor drives. The TC1796 is the first broadly available TriCore-based microcontroller with embedded flash memory; it targets automotive-engine, transmission-control systems, as well as industrial-drive applications. The C166S and TriCore-based TC-1MP synthesizable cores are available in the Synopsys DesignWare Star IP (intellectual-property) program. The Linux-capable TC1130 microcontroller targets industrial and communications applications. The TC1796 meets automotive-power-train and control needs.

▶INFRANT TECHNOLOGIES

Infrant's highly integrated NSPs (network-storage processors) target NAS (network-attached-storage) and media-server-appliance applications. The NSPs enable efficient network-storage devices by integrating Gigabit Ethernet, multiple Serial ATA hard-disk interfaces, and hardware-based RAID (redundant array of inexpensive disks) 0/1/5 redundancy into a single device.

Infrant's second-generation NSPs, the IT3102 and IT3107, target the home-media-server and SOHO (small-office/home-office) NAS markets. The IT3102 embeds two channels of Serial ATA controller, and the IT3107 integrates four. In addition to hardware RAID 0/1/5, the IT3100 supports X-RAID, Infrant's patent-pending expandable RAID technology that enables expansion of the NAS array from one to four drives.

▶INTEGRATED DEVICE TECHNOLOGY

The IDT (Integrated Device Technology) Interprise family of integrated communications processors delivers data processing at line-rate speed with processing headroom for value-added features. IDT based the processor cores on the 32-bit MIPS ISA (instruction-set architecture). Interprise processors and their development tools facilitate designs for SOHO (small-office/home-office) routers, Ethernet switches, WAPs (wireless-access points), VPN (virtual-private-network) equipment, and more.

IDT's RC32434 Interprise integrated communications processor, operating as fast as 400 MHz, targets the digital home network, which includes multimedia applications, such as media servers, media adapters, and IP (Internet-Protocol)-based network appliances. The integrated nonvolatile RAM and an authentication unit for security functions enable digital-content-protection applications and identification storage.

The RC32365 Interprise processor integrates a hardware-accelerated IPsec (IP-security) engine that improves the operating frequency by 20%, to as much as 180 MHz with 70 Mbytes/sec of IPsec throughput. IDT has introduced enhanced versions of the RC32332 and RC32333 processors that offer power reduction.

▶INTEL

Intel offers an extended family of network and communications processors targeting applications with increasing processing demands created by faster line speeds and deeper packet-inspection requirements of content-based services, as well as to support multiple protocols and evolving industry standards. The IXP460 and IXP465 network processors, the latest additions to the IXP4XX product line, offer a higher speed Intel XScale core, expanded connectivity options, and enhancements of end-system reliability and security. The IXP2325 and IXP2350 network processors target network-access and -edge applications by combining data-plane- and control-plane-processing capabilities in a single chip; they are the first network processors Intel has built on 90-nm process technology.

Intel's 64-bit-capable low-voltage Xeon processor operates at 2.8 GHz and has a 800-MHz system bus. It targets storage applications, such as controllers for storage networks. The new processor features Intel EM64T to extend memory addressability of storage systems beyond 4 Gbytes, which eliminates performance penalties associated with large storage applications, such as database programs. Additional introductions include the Pentium M processor 760, Celeron M processor 370, and Celeron M processor ultra-low-voltage 373.

▶MICROCHIP TECHNOLOGY

Microchip bases its PIC microcontrollers, which enable designers to migrate from six- to 84-pin devices among all families with little or no code changes, on the PIC RISC architecture.

Major 8-bit PIC-microcontroller introductions from Microchip this year include the PIC10F, with flash memory, in a six-pin, SOT-23 package. The company integrated two low-pin-count PIC microcontrollers with the Keeloq cryptographic peripheral targeting secure-data-transmission and authentication applications, such as battery-clone elimination. The PIC16F785 makes it easier for power-supply designers to use the programmability of digital control in power-conversion applications by

integrating analog building blocks.

Microchip brought many high-memory/high-pin-count, 8-bit PIC18F microcontrollers to production, including two general-purpose families with 40-MHz operation at 5 and 3V, 128 kbytes of flash, and peripherals in 80-pin packages. Function-specific PIC18Fs include a full-speed USB 2.0 family. An expansion of the CAN (controller-area-network) family combined the ECAN (enhanced-CAN) module and Nanowatt Technology power management inside a 28-pin CAN microcontroller with 64 kbytes of flash memory. The company added eight members to the LCD PIC microcontroller family, including a 28-pin device and programmable 80-pin microcontrollers that can drive 192 segments.

Microchip also introduced wired and wireless embedded-connectivity products. The PICDEM Z 2.4-GHz demonstration kit supports the ZigBee wireless protocol with development hardware and Microchip's free ZigBee stack, which works with PIC18s. The 28-pin ENC28J60 Ethernet controller can connect to any microcontroller via an SPI serial interface (rather than PCI or ISA). Microchip also offers a free TCP/IP stack for all PIC18s.

The dsPIC family of DSCs (digital-signal controllers) features a DSP engine with 30-MIPS nonpipelined performance implemented with a C-compiler-friendly microcontroller architecture and design environment. The 20 dsPIC30FXXXX 16-bit flash DSCs target motor-control, power-conversion, sensor, and general-purpose applications.

Microchip entered 18 dsPIC DSCs into volume production this year, including one it offers in a 636-mm QFN package. This family spans 18 to 80 pins. Microchip offers new software libraries for the dsPIC, many free or available for a one-time fee.

▶MIPS TECHNOLOGIES

MIPS Technologies offers processor architectures and cores targeting digital consumer and business applications. The company licenses its 32- and 64-bit RISC IP (intellectual property) to semiconductor companies, ASIC developers, and system OEMs. Core families include the MIPS 32 4K, 4KE, M4K, 4KSd, 24K, 24KE, and Pro Series processor cores.

MIPS Technologies recently introduced the MIPS32 24KE family of cores—the first to integrate the MIPS DSP ASE (application-specific extension), which the company announced last year. The 24KE core family leverages the high-performance 24K microarchitecture, adds DSP functions, and reduces overall SOC (system-on-chip) die area, cost, and power consumption. The 24KE Pro family supports the CorExtend capability and includes features such as ultrafast multiplication, intelligent caches, and floating-point support, making it suitable for interactive television, set-top boxes, DVD, and other performance-driven applications.

▶NATIONAL SEMICONDUCTOR

National Semiconductor's CP3000 connectivity-processor family combines a RISC core with on-chip SRAM and flash memory, hardware-communications peripherals, and an expandable external bus to target embedded-system-communications applications, such as vehicle-network gateways, hands-free car kits, and industrial/medical instrumentation and control. National Semiconductor's single-chip CP3000 processors feature Bluetooth-lower-link-controller, USB, CAN (controller-area-network), Access.bus, Microwire/Plus, and Advanced Audio interfaces.

The COP8 flash microcontrollers feature an 8-bit core and as much as 32 kbytes of onboard flash that designers can use as data or program storage and work for more than 100,000 delete/write cycles. The devices offer virtual-EEPROM functions, in-system programming, and integrated analog- and mixed-signal functions for stand-alone and Internet-controlled applications.

▶NEC ELECTRONICS AMERICA

NEC Electronics America's 8-bit K0 and K0S families, also available with embedded flash memory, provide low power consumption and integrate peripherals such as LCD drivers and controllers. The microcontrollers target consumer appliances and industrial-control applications. The 32-bit V850 family delivers 32-bit-processing performance, low-voltage operation, DSP functions, and on-chip peripherals targeting consumer-electronics and other embedded-system applications. The 64-bit VR Series MIPS-based microprocessors provide high-performance and scalability targeting embedded systems from Internet and digital consumer devices to servers and switches.

Over the past year, NEC expanded its 32- and 8-bit microcontroller offerings. The company introduced to the V850 family the V850E2/ME3, a 32-bit microcontroller for use in inverters, industrial equipment, printers, and digital consumer products. On the 8-bit side, NEC announced the 78K0/Fx series of microcontrollers for automotive-body applications and the 8-bit 78K0/Kx2 series, featuring embedded flash memory, for use in home appliances, consumer-electronics products, industrial equipment, and sensor applications.

▶NETSILICON

NetSilicon offers processor families based on the ARM 7 and ARM9 cores. It bases the NS9750 and NS9775 on the ARM 926EJ-S core. The NS9750 integrates Ethernet, USB, PCI, LCD, 1284, and serial I/O. The NS9775 is a high-performance color-laser-printer processor and integrates Ethernet, USB, and PCI to improve the cost performance of color laser printers.

▶OKI SEMICONDUCTOR

Oki's Advantage microcontroller family comprises ARM-core based products ranging from the ML671000 with a built-in USB controller to the high-performance, 120-MHz ARM946E-based 6200 Series with instruction and data cache. Oki's 4060, 4050, 675K, and 674K series ARM7 Advantage microcontrollers offer variations in frequencies, memory sizes, cache, features, and packages. Devices in Oki's 675K series have an operating frequency of 60 MHz and 8 kbytes of unified cache; the 674K series operates at 33 MHz. The pin-compatible 675K and 674K series are available with ROMless, 256 and 512 kbytes of flash for easy performance, and memory upgrades.

Oki Semiconductor added a small ARM microcontroller to its product family. Oki's new 4060 series includes a 4.84×5.09-mm, 64-pin wafer-chip-size package with embedded flash, ADC channels, selectable clock gears, and standby modes drawing 25 mA from one 2.5V supply. QFP and BGA packages are also available.

The 6200 series features an ARM9 core with an integrated USB 2.0 and PHY (physical layer) on one chip. The 6200 series, with its ARM946ES core, comprises the ML696201 (ROMless) and the ML69Q6203, which includes 512 kbytes of flash memory. These products feature a high-speed USB 2.0 interface with on-chip MAC (media-access-control) and PHY layers, Ultra-DMA66 hard-drive controller (ATA), NAND flash, and a Smart Media controller.

▶PHILIPS SEMICONDUCTORS

Philips Semiconductors offers 8-, 16-, and 32-bit devices targeting low- to high-end applications in the consumer, communications, computing, medical, connectivity, and automotive industries. The latest offering from Philips is the LPC3000 family of microcontrollers, a 90-nm ARM9-family-based 32-bit microcontroller that Philips based on its Nexperia platform. The LPC3000 family runs at 1V at speeds to 200 MHz. The LPC3000 family features a USB, a real-time clock, a NAND-flash interface, Ethernet, and a vector floating-point coprocessor for full support of single- and double-precision calculations.

Philips based the LPC2100 family on a 1.8V ARM7DMS-S core. The devices

operate as fast as 60 MHz and include a host of peripherals, such as multiple serial interfaces, a 10-bit ADC, and external-bus options. It bases the LPC700 family, targeting applications that demand low-voltage, high-integration, and low-cost, on a high-performance, six-clock 80C51 that executes instructions at twice the rate of the standard 80C51. The LPC900 family targets applications that demand low voltage, high integration, and low cost over a range of performance requirements.

▶PMC-SIERRA

PMC-Sierra's MIPS-based processors target metropolitan transportation, storage-area networking, wireless equipment, VOIP (voice over Internet Protocol), Internet-routing equipment, and enterprise switches, as well as multifunction- and laser-printer applications. The PMC-Sierra family of 64-bit, integrated 1-GHz dual- and single-CPU core devices deliver high performance, low latency, and low power with integrated standard interfaces, including PCI, DDRI and DDRI memory controller, Gigabit Ethernet, and HyperTransport. Pin-compatible devices from 250 to 900 MHz enable seamless performance scalability.

The Multi-Service Processor family, PMC-Sierra's newest MIPS-based offering, targets VOIP-terminal applications, such as wired and wireless terminal adapters, home gateways, and voice-enabled routers.

▶QUICKLOGIC

The QuickMIPS family combines an embedded-processor subsystem and programmable logic on a single die. QuickLogic develops intellectual property and software to target applications that distribute digital media over Internet Protocol networks, including in-car infotainment, digital signage, overhead projectors, and medical imaging. QuickLogic offers modules, such as video compression/decompression, encryption, and digital-rights management. This device architecture provides opportunities for designers to make trade-offs in implementing system functions in hardware for improved performance or in software for increased system flexibility.
QuickLogic's Vialink technology helps protect user-developed IP in the programmable logic from tampering.

▶RABBIT SEMICONDUCTOR

Rabbit Semiconductor offers low-EMI microprocessors for embedded control, communications, and Ethernet connectivity. The Rabbit 3000/2000 processor families feature a glueless architecture and Dynamic C development software. The high-performance, 8-bit Rabbit 3000 processor features LQFP or TFBGA packages, clock speeds as high as 55.5 MHz, ultralow-EMI communication capabilities, support for TCP/IP, 1.8 to 3.6V operation, and 5V-tolerant I/O.

▶RENESAS TECHNOLOGY

Renesas Technology's product portfolio includes 8- to 32-bit microcontrollers and microprocessors targeting embedded-system applications. More than 150 microcontroller offerings operate from 1 to 80 MHz with on-chip flash memories of 8 kbytes to 1 Mbyte. For home appliances, such as white goods, Renesas offers low-power, cost-sensitive 4- to 16-bit microcontrollers in the R8C/Tiny, H8/Tiny, R8/SLP, 740, and 4500 series. Devices in the SuperH and M16C/M32R families target automotive, in-car-navigation, and industrial applications. For PC/server applications, the 16- and 32-bit microcontrollers in the H8 family balance function and performance. The M16C and M32 families target consumer applications, and Renesas' AE series chips smart-card platforms have 68 kbytes of EEPROM and a 1024-bit encryption coprocessor.

Renesas introduced three new groups of devices in the low-pin-count, small-package R8C/Tiny series that suit cost-sensitive applications; these 16-bit microcontrollers feature clock oscillators, power-on-reset and low-voltage-detect functions, and 10-bit ADCs. They can act as the main processors in appliances or as subprocessors in large systems. Two 32-bit, 50-MHz microcontrollers, the H8SX/1653F and H8SX1651, have a serial communication interface that handles both asynchronous and clock-synchronous data transfers and enables them to target PC peripherals and point-of-sale terminals.

Targeting automotive systems, M16C/29 microcontrollers offer as much as 128 kbytes of flash memory and a CAN (controller-area-network) Version 2.0B interface; they produce low levels of EMI and withstand high levels of EMI from external sources. For in-vehicle navigation and infotainment systems, the SH7080 32-bit RISC microprocessor uses a 400-MHz SH-4A CPU core that delivers 720-MIPS, 2.8-GFLOPS performance. It supports advanced functions, such as speech recognition and synthesis without an external DSP.

▶SAMSUNG ELECTRONICS

Samsung's S3C2410 and S3C2440 minimize system cost and eliminate the need to configure additional components by featuring common peripherals for mobile-system applications, such as wireless handheld devices, smart phones, and GPS (global-positioning-system)-enabled portables. These processors feature a 16/32-bit ARM920T RISC core. Samsung developed the processors using CMOS-standard cells and a memory compiler, and both adopt the AMBA (Advanced Microcontroller Bus Architecture). Both processors include a built-in NAND flash boot loader, and they support WinCE, Palm, Symbian, and Linux operating systems.

▶SHARP MICROELECTRONICS

Sharp's ARM-based, 16- and 32-bit BlueStreak microcontrollers range from ARM7 devices for cost-conscious applications, to high-performance ARM9 devices for media-rich environments. The 16/32-bit ARM7 BlueStreak microcontrollers feature on-chip SRAM, a color and gray-scale LCD controller, CAN (controller-area-network) 2.0B, and a low-voltage detector that enables them to target applications such as GPSs (global-positioning-systems), PDAs, printers, copiers, security-control panels, and smart appliances. The 32-bit series of BlueStreak microcontrollers feature cache, an MMU, a color-LCD controller, SRAM, a DMA controller, infrared support, pulse-width modulators, and an on-chip PLL. The ARM9 LH7A400 and LH7A404 add USB and MMC to target handheld devices, such as GPSs, games, PDAs, and pocket PCs.

▶SILICON LABORATORIES

Each of Silicon Laboratories' 8-bit mixed-signal microcontrollers integrates high-performance analog peripherals; a high-speed, pipelined 8051 CPU; ISP (in-system-programmable) flash memory; and on-chip JTAG-based debugging. All of Silicon Labs' processors feature in-system debugging, eliminating the need for an emulator.

Silicon Labs' single-chip USB products integrate a full-speed USB 2.0 function controller and on-chip clock recovery. Silicon Labs' single-chip CAN (controller-area-network)-bus products integrate a CAN 2.0B controller and high-performance ADCs. The precision mixed-signal microcontroller family combines high-precision analog data converters from 10 to 24 bits of resolution with a high-throughput 8051 CPU targeting analog and computationally intensive applications. Silicon Labs' small-form-factor family of microcontrollers packs the benefits typical of the company's microcontroller line into small micro leadframe packages.

Over the past year, Silicon Labs announced the CP2102, a small and highly integrated, single-chip USB-to-UART bridge. The CP2102 simplifies the upgrade from RS-232 to USB by including royalty-free drivers that eliminate the need for additional software. Silicon Labs also announced its entry into the short-range-

wireless market with the 802.15.4 and ZigBee development kits. Silicon Labs' ZigBee-ready devices leverage precision mixed-signal microcontrollers that combine high-precision analog peripherals and a high-throughput 8051 CPU with flash memory targeting wireless automation, industrial, medical, and residential-monitoring and -control applications.

▶SILICON STORAGE TECHNOLOGY

Silicon Storage designs and manufactures various densities of flash-memory components, flash mass-storage products, and flash microcontrollers targeting the digital-consumer, networking, wireless-communications, and Internet-computing markets. SST's flashFlex51 family of 8-bit, Superflash CMOS microcontroller products implements the 8051 architecture and instruction set. These microcontrollers include in-application-programming and hard- and soft-lock security features. The flash-Flex51 microcontrollers target the high-reliability, high-flexibility, low-voltage, and low-power requirements of today's computer peripherals, communication equipment, digital consumer/appliances, and networking applications.

▶STMICROELECTRONICS

STMicroelectronics offers 8-, 16-, and 32-bit microcontrollers and microprocessors, including a family of ARM7-based microcontrollers, and application-specific devices for motor control, USB, and CAN (controller-area-network) applications. The 8-bit portfolio includes the "bulletproof" ST6 family, the 8051-based microPSD family, and the ST7 family. Other devices include the ST7MC, for controlling three-phase brushless motors, and a 3V version of the ST72324 general-purpose microcontroller. New devices include a turbo-plus version of the microPSD. The ST9 family represents high performance at low costs for 8- and 16-bit-device applications.

The company offers 16-bit devices with the ST10 family, which includes devices operating as fast as 50 MHz with a four-stage pipeline. The 32-bit STR-ARM family, based on the ARM7 core, supports the Thumb 16-bit ISA (instruction-set architecture) and features peripherals such as USB, CAN, and buffered SPI. The SH4-based ST40 is available as a standard product for high-performance applications. For x86 designs, the STPC is available in several configurations to provide PC-on-chip systems to take advantage of x86 software.

▶STRETCH

The Stretch S5000 family of software-configurable processors, based on the S5 engine, boosts system performance by enabling customized acceleration through the embedded programmable logic within the processor engine. The processors' design architecture and methodology merge the software model of general-purpose processors and the parallelism and flexibility of programmable logic to deliver customizable acceleration. The Stretch S5 engine, which powers every S5000 processor, integrates the Stretch ISEF (instruction-set-extension fabric) with the Tensilica Xtensa RISC-processor core. With Stretch's proprietary technology, developers use C/C++ to program the processor and "configure" the ISEF with custom instructions. Designers can tailor Stretch processors to address computationally intensive applications in markets such as high-end consumer electronics, medical imaging, telecom, networking, and military.

This year, Stretch completes the introduction of the S5000 family with the release of the S5620 and S5500 software-configurable processors. Based on the Stretch S5 engine, each processor incorporates a 300-MHz, 32-bit Xtensa core with integrated programmable logic; embedded memory; and peripherals targeting high-performance, computationally intensive applications. The S5620 offers performance enhancements to systems using PowerPC-based processors in applications in which computational-function offloading is critical.

▶TENSILICA

Tensilica licenses the Xtensa V and Xtensa LX processor cores. The Xtensa V is Tensilica's configurable and extensible 32-bit RISC processor. The Xtensa 32-bit architecture features a compact instruction set for embedded-system designs. The basic architecture has a 32-bit ALU; as many as 64 general-purpose physical registers; six special-purpose registers; and 80 basic instructions, including compact, 16- and 24-bit, rather than 32-bit, RISC-instruction encoding.

Tensilica introduced the Xpres (Xtensa PRocessor Extension Synthesis) compiler for Xtensa LX only. The Xpres synthesis tool creates tailored processor descriptions for the Xtensa LX processor from native C/C++ algorithms. For small algorithmic kernels, the Xpres compiler explores potential configurations in just minutes. For large application programs, the Xpres compiler can explore millions of potential combinations of processor configurations in less than an hour. It supports fine-tuning-control options that are fully integrated into the Xtensa Xplorer design environment.

The Xtensa LX adds I/O and computational performance to the basic Xtensa V architecture. It implements Tensilica's Flix (flexible-length-instruction-extension) architecture, which is a configuration option that allows designer-defined instructions to comprise multiple independent operations bundled into a 32- or 64-bit instruction word. The LX seamlessly intermixes wide, 32- or 64-bit Flix formats with the base Xtensa instruction-set architecture's 16/24-bit instructions.

▶TEXAS INSTRUMENTS

TI's MSP430 platform of ultra-low-power, 16-bit RISC microcontrollers targets battery-powered measurement applications and enables systems to simultaneously interface to analog signals, sensors, and digital components. The architecture features power consumption at 0.1 mA for RAM retention, 0.8 mA during real-time-clock mode, and 250 mA/MIPS while active. Key target applications include utility metering, portable instrumentation, and intelligent sensing.

The new MSP430F2xx microcontroller family provides twice the processing performance and half the standby power consumption of earlier devices. Devices feature a real-time-clock-standby mode of less than 1 mA with the ability to switch in less than 1 msec to a fully synchronized 16-MIPS active mode. Low-power standby current and instant-on active mode enable designs using smaller, lower cost batteries in applications such as portable medical instruments and security systems.

The new low-cost, signal-chain-on-a-chip MSP430F42x0 microcontroller targets high-precision sensing and measurement applications.

New, general-purpose TMS470 32-bit RISC ARM7TDMI-based microcontrollers feature single-cycle access to embedded flash at as much as 60 MHz in pipeline mode and support high accuracy for timing functions using a programmable, 32-channel, high-end timer. The TMS470 includes a leading multibuffered, 10-bit ADC with a 1.55-msec conversion time as well as enhanced CAN (controller-area-network) controllers that offload the CPU for a higher system performance.

▶TOSHIBA AMERICA ELECTRONIC COMPONENTS

Toshiba offers highly integrated, 8-, 16-, and 32-bit CISC microcontrollers and a family of 32- and 64-bit MIPS-based RISC microprocessors.

Toshiba this year rounded out its microcontroller product offerings with low-power, LCD-type embedded flash microcontrollers targeting heating and metering applications. Toshiba announced the development of NANO flash in the 32-bit TMP19A43-

FDXBG, which combines high-density embedded memory with ultralow power consumption. Toshiba launched the TX4939XBG-400, its first embedded PCI-based processor using 90-nm process technology; it targets digital-consumer applications. Toshiba also introduced the TX9956CXBG; operating at 533 or 666 MHz, it targets multifunction printers and high-end set-top-box applications.

Continuing to execute on its strategy to offer focused platforms, Toshiba introduced the AVM49R TX System RISC multimedia reference platform for IP (Internet Protocol) set-top box, digital-multimedia appliances, and home gateways.

▶TRANSMETA

Transmeta develops and offers computing technologies that improve performance, reduce power consumption, and control heat generation in electronic devices. The company deploys its technology and IP (intellectual property) through licensing, synergistic engineering services, and customized processor development, using a unique partnership model. Transmeta's x86-compatible, software-based microprocessors target high-volume applications that demand high performance, energy efficiency, and x86-software compatibility. Transmeta also develops advanced power-management technologies for controlling leakage and increasing power efficiency in semiconductor and electronic devices.

The Efficeon processor targets power-efficient x86 applications by featuring a 256-bit-wide VLIW (very-long-instruction-word) engine that can execute as many as eight instructions per clock cycle; a 1-Mbyte L2 cache; and support for MMX (multimedia extension), SSE (streaming-single-instruction-multiple-data-extension), SSE2, and SSE3 instructions.

▶UBICOM

Ubicom offers wireless-network processors that can implement communication and control functions in software, so that one processor can support many device interfaces and protocols. All IP2022 family products are deterministic and use an enhanced, four-stage-pipelined Harvard architecture. The devices feature single-cycle instruction execution and a fixed, deterministic three-cycle interrupt response time.

On-chip program memory for the IP2022 family comprises reprogrammable flash with additional instruction SRAM to deliver fast access and high processor performance. Ubicom's previous-generation IP2022 processor runs at 120 MHz and targets wired- and wireless-networking applications. The processor also implements I/O in software and features single-cycle instruction execution; deterministic operation; on-chip flash and RAM; and flexible, general-purpose I/O.

Ubicom's IP3000 family devices drive high-data-rate standards and multifunction wireless devices. The first family member, the IP3023-250, targets high-performance network devices or 802.11a/b/g-infrastructure equipment, such as routers, bridges, and access points. The devices feature single-cycle instruction execution and a fixed, deterministic, three-cycle interrupt response time.

The IP3023 processor targets SOHO (small-office/home-office) wireless-system applications and can operate as eight separate processors running at speeds as high as 250 MHz in 3.9-MHz increments by providing eight-way multithreading and zero-cycle context switching between the threads. For wireless-networking applications, the IP3023 can deliver, without data compression, line-speed NAT (network-address-translation) routing on 10/100 Mbps of real data throughput with 802.11 a/g radio chip sets using turbo mode.

▶VIA TECHNOLOGIES

Via offers power-efficient processors for the x86 personal-electronics and embedded-device markets with a range of feature-rich Via digital-media chip sets. Via divides its processors into five product families that it bases on power consumption and performance criteria ranging from fanless operation to power-saving capabilities for battery-operated mobile devices: the Via C7 and Via C7-M (Mobile), fanless Via "Luke," Via Eden-N, fanless Via Eden ESP, Via C3-M (mobile), and Via C3 processors.

▶XEMICS

Xemics offers 8- to 22-bit microcontrollers that interface sensors and radio transceivers and target autonomous battery-operated wireless devices. These devices operate at a constant one instruction per clock that is independent of the type of operation and addressing mode. The dedicated interface blocks; high-resolution, preamplified ADC; and transceiver serializer/deserializer all enable miniature wireless-sensing applications, reducing the bill-of-materials costs by eliminating external components.

The Radio Machine device for ISM (industrial, scientific, and medical)-band transceiver interfacing, includes a low-power RISC core with the BitJockey, a serial interface for radio protocols, and a UART. The Sensing Machine device for sensor interfacing includes a low-power RISC core with the ZoomingADC and a high-resolution sigma-delta ADC with a programmable preamplifier.

▶XILINX

Xilinx offers processor and silicon platforms that enable designers to optimize performance and prices for their applications. The PowerPC 32-bit core is immersed (hard) in the Virtex family of FPGAs. New offerings include dual 32-bit embedded PowerPC processors running at 450 MHz on the Virtex-4 FX platform. New features include an integrated APU (auxiliary-processor-unit) controller and dual integrated trimode Ethernet MACs (media-access controllers). The APU enables designers to extend the native PowerPC instruction set and improve software-algorithm execution with application-specific hardware accelerators implemented in the FPGA logic.

The 32-bit, configurable, general-purpose RISC MicroBlaze soft core processor is available with Spartan and Virtex-platform FPGAs. The latest version of the Xilinx MicroBlaze 32-bit configurable soft-processor core delivers a 25% increase in core performance over previous versions. In addition, MicroBlaze includes a tightly integrated FPU option, user-configurable hardware options, and optimized debugging logic. The 8-bit PicoBlaze microcontroller can target Spartan FPGAs and CoolRunner CPLDs.

▶ZILOG

Zilog provides 8-bit micrologic semiconductors for embedded control and communication applications in markets such as consumer electronics, home appliances, security systems, POS (point-of-sale) terminals, PC peripherals, industrial, and automotive. Zilog has four families of microprocessors: The Z8 and Z80 are its legacy microprocessor architectures, and the Z8 Encore! and eZ80 Acclaim! are next-generation microprocessor architectures. In most of its micrologic devices, a microprocessor joins with ROM, OTP (one-time-programmable), or flash memory. The company also sells a stand-alone, general-purpose Z80 microprocessor that does not integrate memory.

Zilog continues to focus on the 8-bit-system market, adding application-specific features that target universal-remote-control, home-appliance, computer-peripheral, security, sensor, and industrial-automation applications. Zilog extended the Z8 Encore! XP family with an eight-pin device that includes the on-chip features and functions of its larger counterparts. It also this year launched the Z8 Encore! GP323 family of low-cost, low-power, general-purpose microcontrollers. Zilog continues to extend the Z8 Encore! and XP families to include additional flash-memory options. It also extended the Crimzon microcontroller family to include additional ROM versions.EDN

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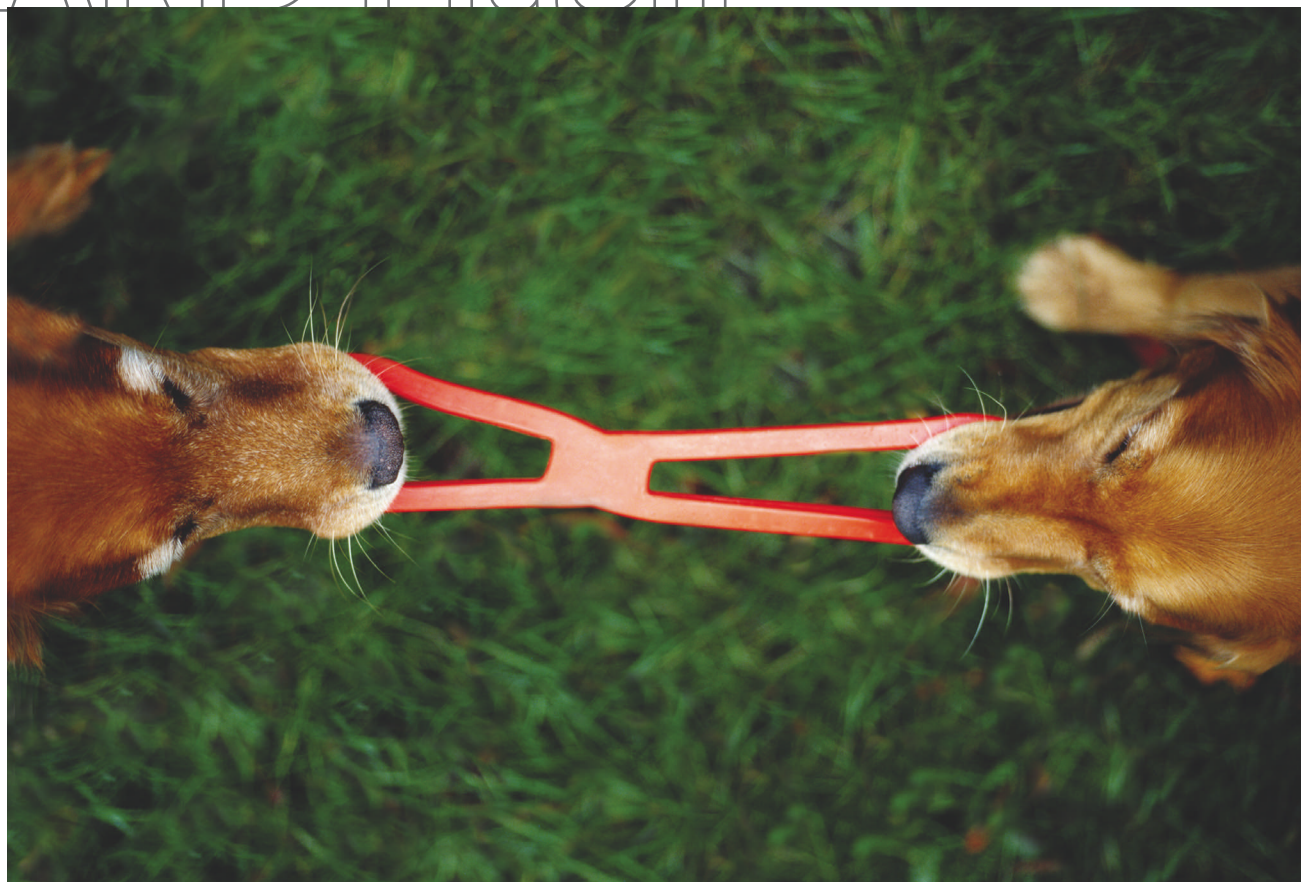

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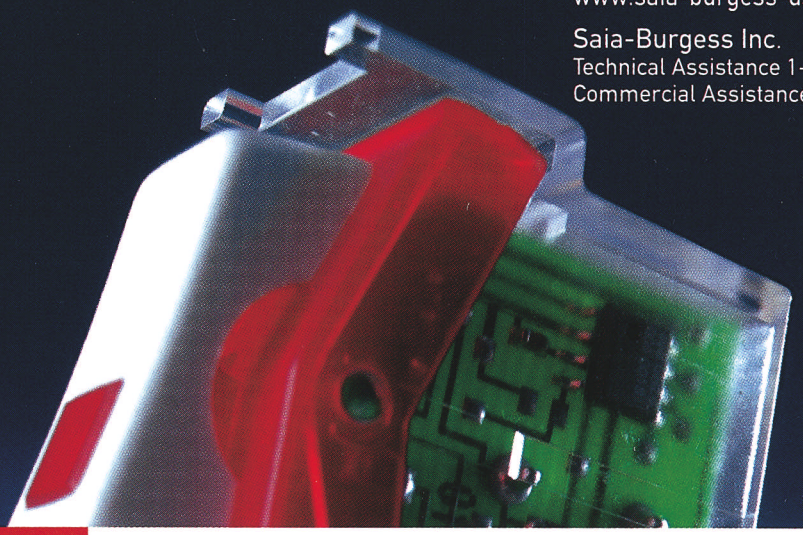

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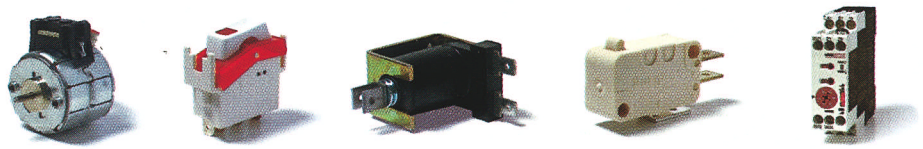

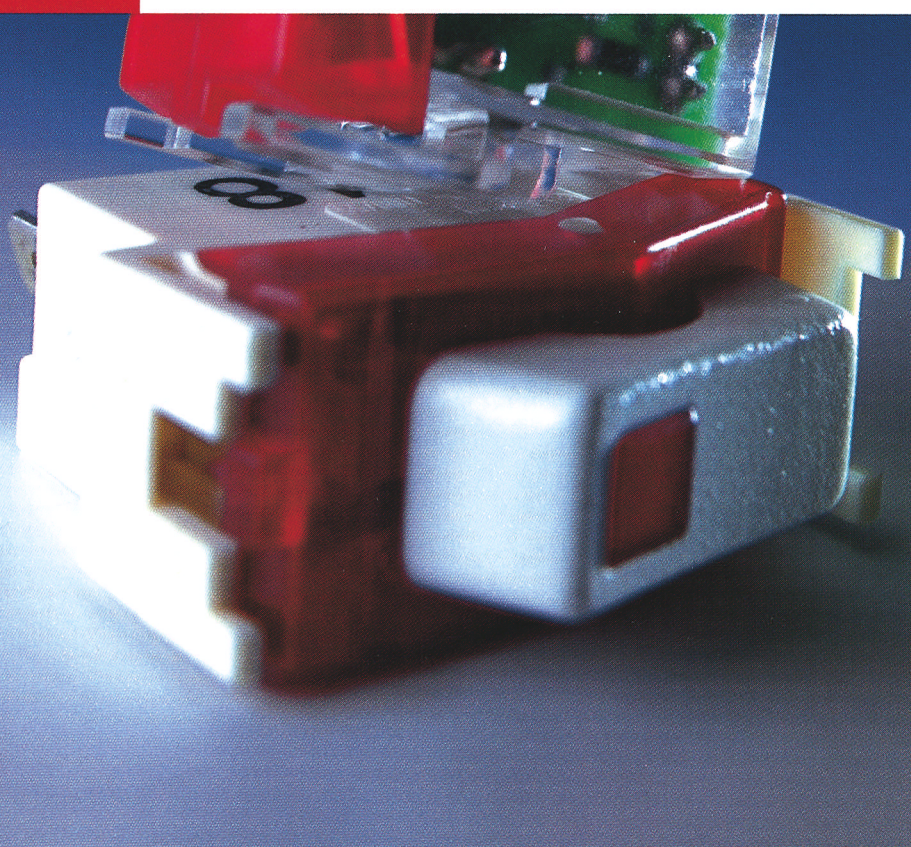

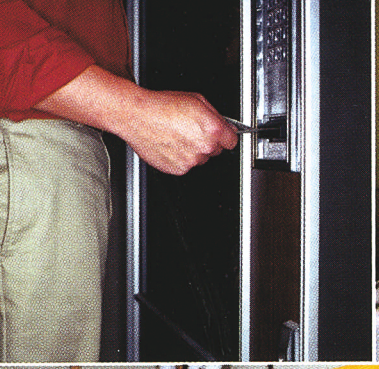

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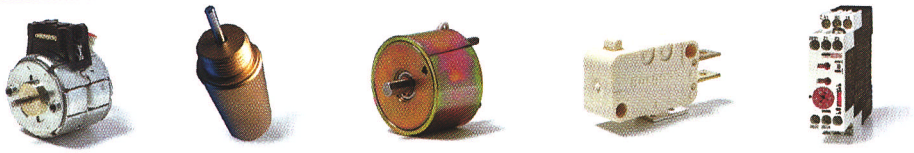

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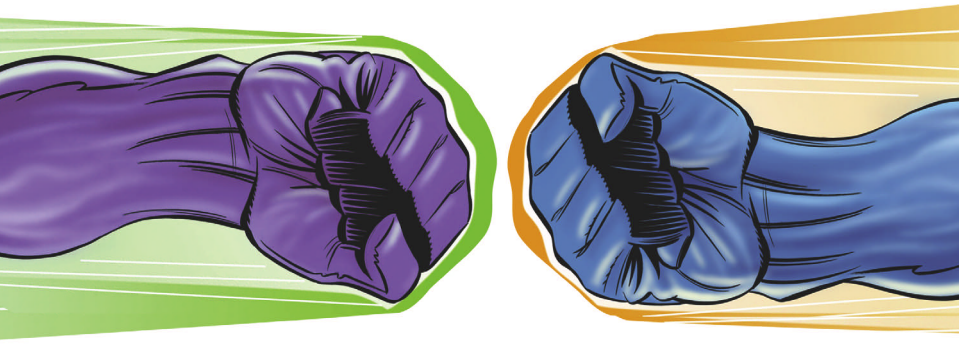

BY RICHARD A QUINNELL • CONTRIBUTING EDITOR

WiFi and Bluetooth fight for bandwidth

BLUETOOTH AND WLAN ARE ON A COLLISION COURSE—NOT IN THE MARKET, BUT IN THE AIRWAVES.

WLAN (wireless LAN) using the WiFi (Wireless Fidelity) IEEE 802.11b/g protocol is becoming standard in PCs and laptop computers, and it is making its way into PDAs and other portable data appliances. At the same time, Bluetooth is arising as a wireless-serial-cable replacement for headsets and microphones in all kinds of mobile-system applications. They are not exactly market competitors, but they share the same frequency band, and, without careful design, that scenario means trouble.

Both wireless protocols operate in the 2.40- to 2.48-GHz ISM (industrial, scientific, and medical) RF band. WiFi uses one of 12 overlapping channels of 22-MHz bandwidth each, and Bluetooth frequency-hops among 79 1-MHz channels evenly spaced across the band. As a result, no matter which channel of WiFi is in use, a risk exists of interference between the two that will result in lowered data throughput for both.

To characterize the impact of this interference, Texas Instruments in 2000 performed a series of tests that measured the throughputs of both WiFi and Bluetooth links in the presence of interference from the other. The results indicate that the distance between the interfering transmitter and the affected receiver strongly influences the impact (**Figure 1**).

In the case of WiFi, a separation of 10m results in minimal impact for short-range WiFi use, with increasing impact over longer ranges. A separation of only 2 cm, as might occur when an interfering transmitter is in an adjacent PCMCIA card slot in a laptop computer, has a much more profound impact. In that situation, Bluetooth can shut down WiFi for all but short-range use.

In the case of Bluetooth, the effect is different. WiFi has minimal impact on Bluetooth when separated by 10m, regardless of range. A 2-cm separation, however, drastically reduces Bluetooth throughput even for short ranges and quickly shuts it down with increasing range.

To mitigate this impact, the Bluetooth community developed AFH (adaptive frequency hopping), which can automatically avoid such interference. AFH causes the Bluetooth link to selectively remove from the hopping sequence those channels on which interference is present (**Figure 2**). The result is that Bluetooth can automatically alter its use of the spectrum to avoid an active WiFi channel. To implement the approach, however, the Bluetooth community needed to convince the FCC (Federal Communications Commission) to change its rules. The FCC has finally approved those changes, and Bluetooth 1.2 implementations can now use AFH.

Unfortunately, AFH does not provide a complete solution to making WiFi and Bluetooth work together in harmony. "AFH gets you only partway there," says Andre Parolin, director of wireless data products at SiGe Semiconductor. "It is there for interference, not coexistence."

More recent testing shows that AFH succeeds in virtually eliminating interference when more than 2m separate the interfering transmitter and the affected receiver, but throughput for each link degrades rapidly with less separation. This situation is currently good enough. Bluetooth's initial market has been in wireless headsets for cell phones. Too few situations arise today in which a user is on a cell-phone call while trying to use a laptop computer connected to a WLAN to consider the interference much of a problem. Changes in the market, however, will once again raise the specter of interference.

The problem comes in emerging applications, such as VOWLAN (voice over WLAN) on laptop computers, cell phones, and PDAs, in which both Bluetooth and WiFi will need to operate simultaneously in the same device. Such applications are becoming more common. The United States, for instance, is adopting WLAN in cell phones to improve coverage, whereas Europe is using it for high-bandwidth downloads to smart phones. In addition, industry analysts expect VOWLAN to become popular in enterprise installations. A survey by market-research company In-Stat/MDR shows that 10% of businesses surveyed use VOWLAN handsets, and 48% are considering implementing VOWLAN.

These trends greatly increase the like-

AT A GLANCE

- Bluetooth and WiFi share a frequency band and interfere when too close.
- Market demands are pushing to include both Bluetooth and WiFi in handheld instruments.
- Bluetooth's adaptive frequency hopping (AFH) will substantially mitigate interference beyond 2m but is inadequate at closer distances.
- Other coexistence approaches are available, the best of which arise when the two MAC layers communicate to arbitrate spectrum usage. Manufacturers that offer ICs for both links are in a position to offer such coexistence options.

lihood of manufacturers implementing Bluetooth and WiFi in the same handset device. With both carrying voice data, neither can afford a major reduction in bandwidth. Yet, in the case of implementing both links in the same handset, maintaining a separation of 2m becomes impossible, and Bluetooth AFH becomes inadequate as a stand-alone approach.

Fortunately, chip-set and other vendors are making available several other coexistence approaches. Some are collaborative, requiring communications between the WLAN and Bluetooth devices to coordinate their actions. Others are noncollaborative, able to operate independently in one or both links. Each approach has its benefits and limitations, although the noncollaborative approaches are better for situations in which only one link is carrying voice traffic.

NONCOLLABORATION

One noncollaborative technique that can reduce the impact of interference is APSS (adaptive packet selection and scheduling) in the Bluetooth link. Bluetooth provides a range of packet types with various payload lengths and FEC (forward-error-correction) options. By adapting the packet types and transmission timing to the channel condition of the current hop, the Bluetooth system can reduce data loss due to interference. Using shorter packets, for instance, reduces the amount of data that the device needs to resend when interference occurs and can improve throughput compared with that of larger packets.

Dropping the use of FEC in Bluetooth when a WiFi system is the cause of interference can also help. Because the packet loss is due primarily to collisions rather than random noise, the FEC overhead adds no significant value. Dropping it thus reduces overhead and increases data throughput.

Developers can implement the APSS technique predominantly in the MAC (media-access-control) layer, keeping the hardware structure virtually unchanged. Several channel-condition-estimation methods are available, including BER (bit-error-rate) and PER (packet-error-rate) profiling. By maintaining a frequency-usage table at the master and slave nodes, with the slave node's updating the master's table every update interval, the systems can also estimate the interference present. By scheduling master/slave transmissions on only the "good" frequencies, the system can avoid the interference, although a possibility of collisions still remains. This technique does have a surprising benefit, however: It saves power because little transmission time goes to waste in a bad channel.

The APSS technique reduces overall throughput by waiting for clear channels, but that situation may not be a problem in many applications. One application in which you cannot use APSS, however, is for handling SCO (synchronous-connection-oriented) voice-data packets. These packets cannot be delayed, waiting for a good channel, without compromising voice quality. Thus, APSS is an inappropriate technique for Bluetooth voice applications.

COLLABORATIVE TECHNIQUES

Collaborative techniques for mitigating interference are alternative approaches that can function when you in some way coordinate the operation of both the Bluetooth and the WiFi channels. One simple example is to control operations at the driver level and to switch between the two radio devices to prevent one from func-

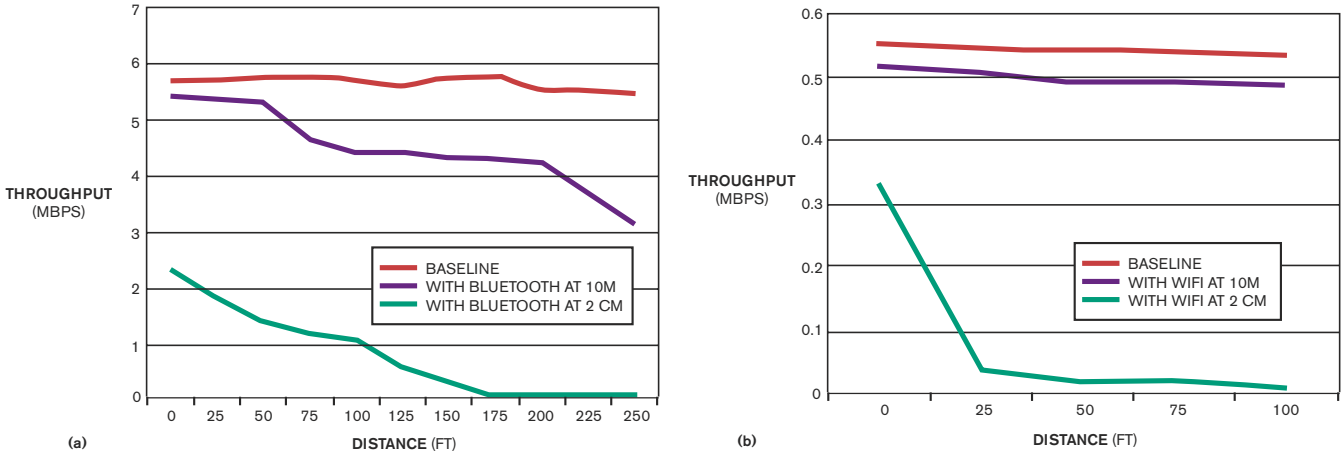

Figure 1 The data rates of WiFi suffer whenever Bluetooth is operating, especially if Bluetooth is close by (a). Bluetooth, however, sees little degradation unless the WiFi transmitter is close (b, courtesy Texas Instruments).

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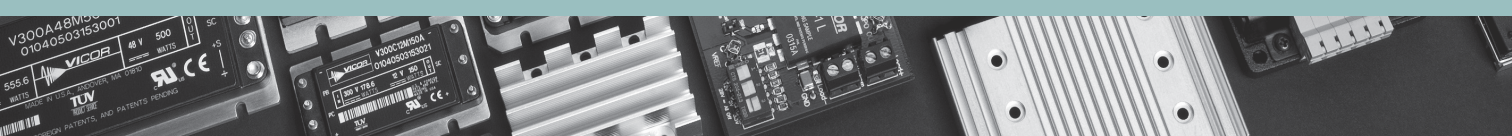

tioning when the other is transmitting. This simple technique severely reduces throughput for both links, however.

Coordination is also possible at a hardware level when both the Bluetooth and the WiFi devices can communicate with each other. Such communication is possible among chips from different manufacturers only when a standardized means of communications is available. Such standards do not currently exist, although the IEEE 802.15.2 task group is developing recommended practices for resolving Bluetooth and WiFi interference. In the absence of such standards, developers should consider proprietary offerings from companies such as Broadcom, Intel, STMicroelectronics, and Texas Instruments that manufacture both types of devices.

One simple collaborative technique is the use of AWMA (alternating-wireless-media access). In this technique, higher level software partitions the WLAN beacon-to-beacon interval into two time segments. One is dedicated to the WLAN, and the other is dedicated to the Bluetooth signal. The Bluetooth device then restricts its transmissions to its allocated time segment. This approach prevents the two devices from interfering with each other.

For this technique to work, the WLAN and Bluetooth devices must be connected, implying that they are collocated in the same physical unit. In addition, all nodes in the WLAN must connect to the same access point so that they are synchronized. The WLAN node in the unit with the Bluetooth device signals the Bluetooth device over a wired connection when the medium is free of traffic, and the Bluetooth device controls the timing allocation. The Bluetooth device must be in its master mode.

As with APSS, this technique does not guarantee a Bluetooth slave timely access to the channel. The slave device can transmit only if it receives permission from the master, and the master must wait until the WLAN node signals a free channel. This approach makes for uncertain timing. Even if the WLAN master tries to allocate time for the Bluetooth transmissions, it cannot control other WLAN nodes in the network. As a result, timing is uncertain, and the technique cannot support SCO voice-data transmissions.

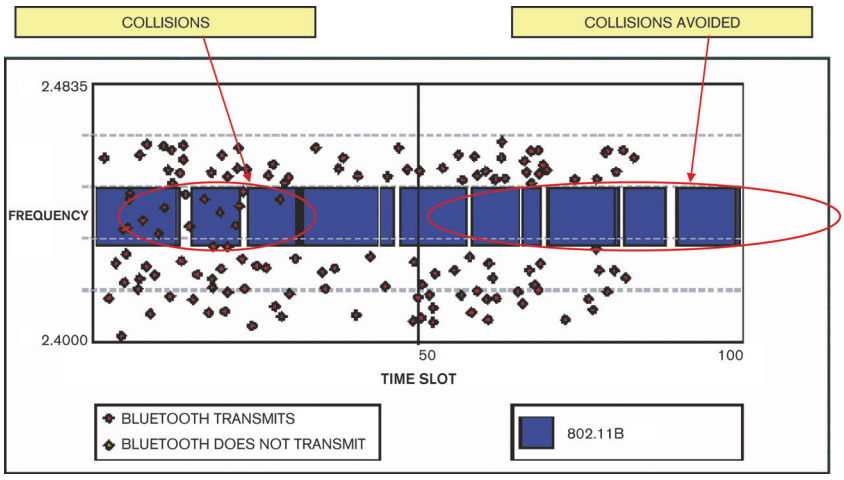

Figure 2 Adaptive frequency hopping uses features available in Bluetooth 1.2 to restrict transmissions on channels on which another transmitter is occupying a fixed bandwidth. The result is fewer collisions and greater throughput (courtesy STMicroelectronics).

VOICE DURING INTERFERENCE

One technique that does support voice is PTA (packet-traffic arbitration), which uses the MAC layer to control traffic. The PTA technique uses a control entity that receives per-transmission transmit requests from each network stack and issues transmission-confirmation signals to the stacks to indicate whether the transmission can proceed. The networks exchange these discrete signals for every packet-transmission attempt.

This technique removes many of the restrictions inherent in other collaborative techniques. For one, it does not require that either network device be a master device. The PTA controller can simply deny any requests that would result in a collision. Because the controller can assign priorities based on packet-traffic classes, it can ensure that Bluetooth SCO packets receive timely handling.

Implementing the PTA approach requires a number of status signals from the two wireless devices in addition to the transmission-request and -confirmation signals. The controller needs to know the traffic priority of each packet, as well as status information from the wireless MAC layer. In addition, it needs to know the Bluetooth frequency in use to determine whether a collision is likely. This additional information requires at least two

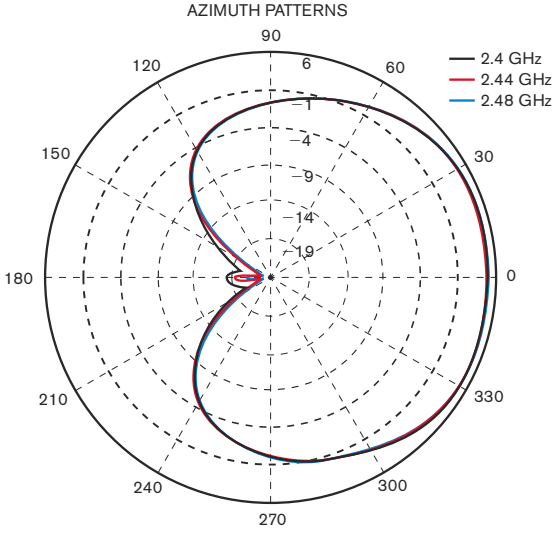

Figure 3 Instead of using an omnidirectional antenna, InterDigital gives developers a means of creating a directional-antenna pattern to reduce the magnitude of interference from collocated transmitters.

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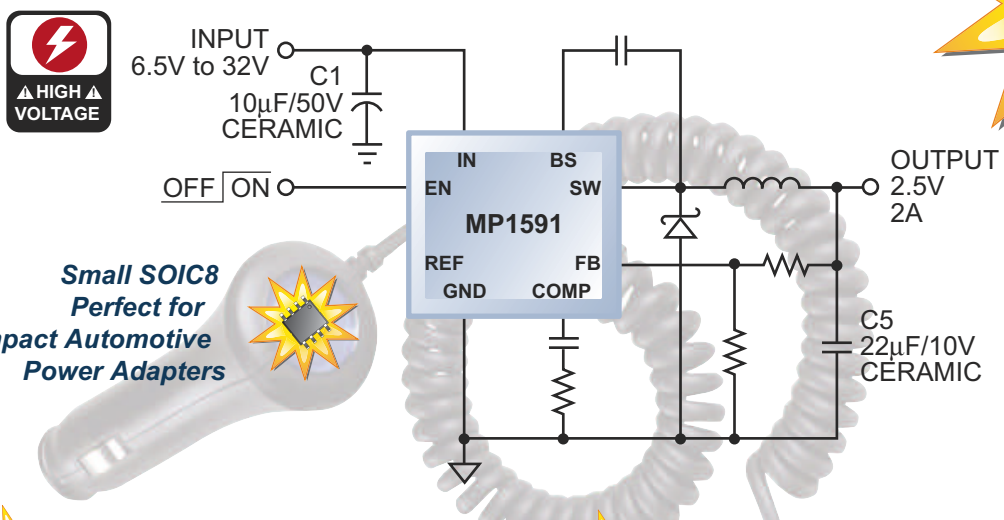

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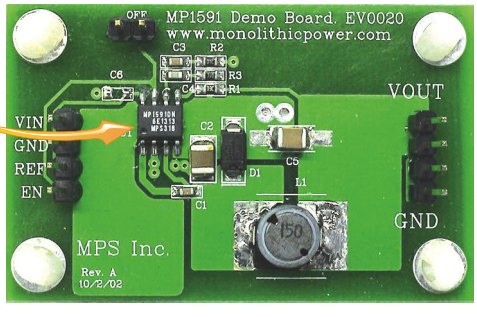

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additional wires to communicate.

Clearly, implementing the PTA approach carries a high potential for dramatically reducing the impact of collocation for Bluetooth and WiFi transmitters. Its complexity and need for special signaling, however, mean that designers can implement the approach only when the hardware designs of the two wireless chips are compatible. Developers seeking to use this method will do best obtaining hardware and PTA software support from a single vendor.

OTHER POSSIBILITIES EXIST

Other interference-reduction techniques are possible. One is to control the direction of the antennas in use. InterDigital, an RF-component company, has developed AIM (adaptive-interference-management) technology that can enable WiFi networks to adapt their operating frequencies in response to interference. The company's AIM PerformWare, which it implements in WLAN routers and access points, allows them to automatically select the optimum operating channel in the presence of interference.

The company also offers an AIM antenna. Most wireless systems today use an omnidirectional antenna. The AIM antenna uses beam forming to create a directional antenna that has a strong null in one direction (**Figure 3**). The approach allows the system to switch among omnidirectional and two opposite-pointing directional antennas to find the pattern that minimizes interference. This approach can extend the effective distance between the WiFi and Bluetooth antennas in a device, allowing Bluetooth AFH to handle the remaining interference effects.

Designers can also mitigate the effects of interference. At the receiver end of a Bluetooth voice transmission, for instance, the receiver can apply error-concealment techniques, such as pitch-period error concealment, to remove some of the artifacts of packet loss in the received speech. Designers can also employ adaptive-interference cancellation at the PHY (physical) layer. Such techniques cannot handle significant interference and data loss, but they can smooth out minor problems.

It may even become possible to completely avoid the problem. The Bluetooth SIG (Special Interest Group) is working with supporters of UWB (ultrawideband) technology to define how Bluetooth can use the greater signal-bandwidth opportunities that UWB provides. If the two successfully merge, the interference issue may disappear.

Another vanishing trick might be to simply eliminate Bluetooth. In the opinion of Fanny Mlinarsky, chief technical officer for test-system vendor Azimuth Systems, WiFi can simply replace Bluetooth. "Bluetooth isn't simpler than WiFi; it simply has lower power. So, simply turn down the WiFi power and use the same data rate, and you'll get the same power as Bluetooth. WiFi has the volume and pricing advantage."

For now, however, if Bluetooth and WiFi must coexist, combining mitigation techniques with more active interference mitigation is the best choice. The techniques that designers can apply depend on the chip sets in use, but the greatest flexibility comes from devices that can coordinate their activities. Whichever techniques developers use, however, the result is a design that produces a more satisfactory user experience when WiFi and Bluetooth operate simultaneously. EDN

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AUTHOR'S BIOGRAPHY

Contributing Editor Richard Quinnell was a practicing engineer, designing embedded systems for more than 15 years. He then switched to covering high technology for the last 15 years.

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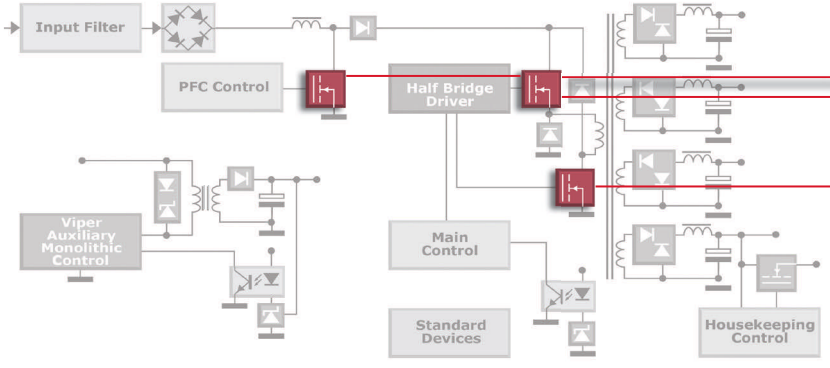

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STB25NM60N	650V	< 0.170Ω	20A	D^2PAK

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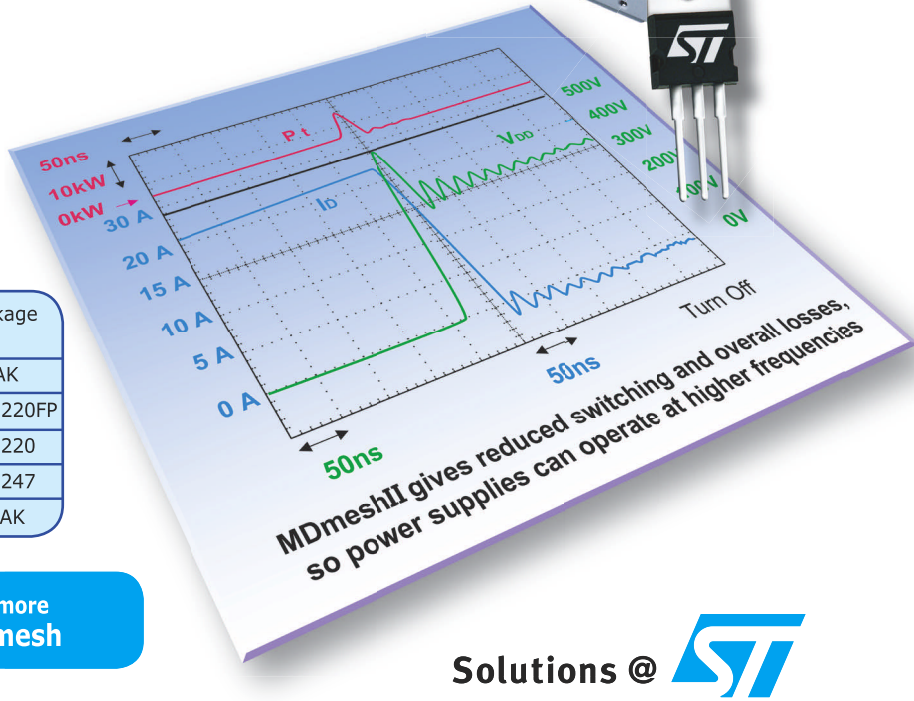

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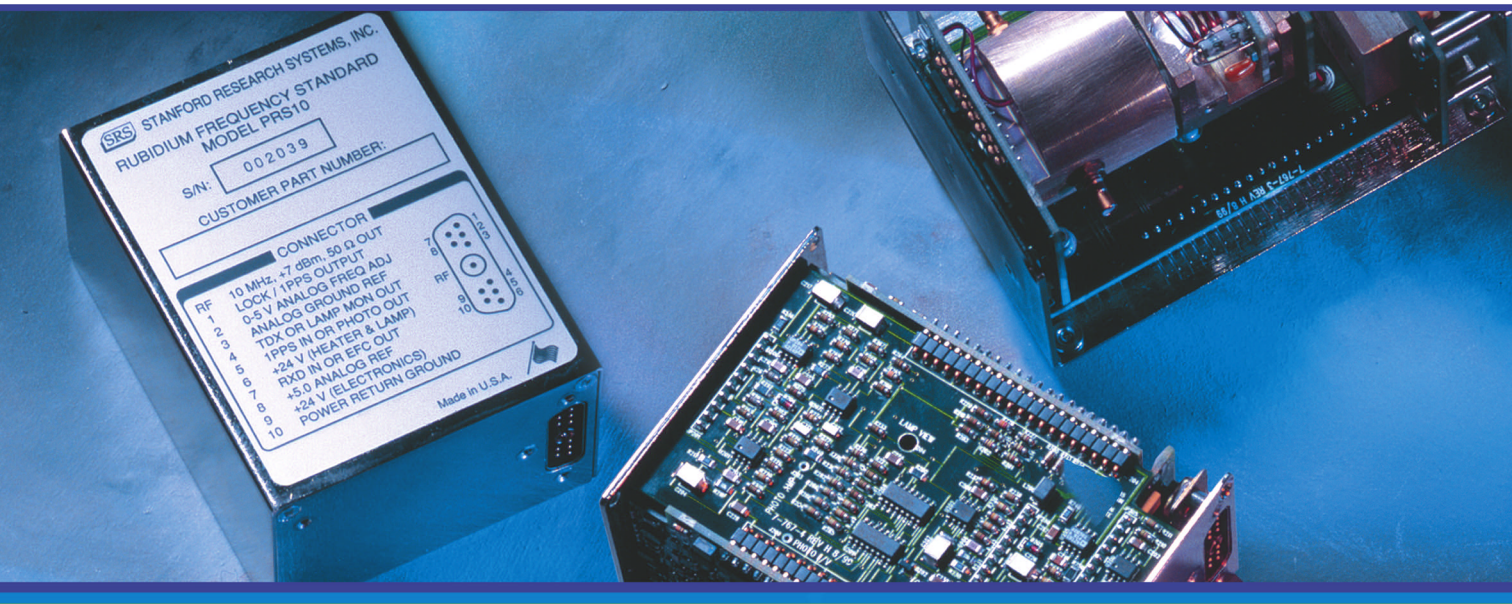

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BY VICTOR ECHEVARRIA • RAMBUS

Choosing and using microprocessor memory interfaces

DESIGNERS EVALUATING MEMORY-INTERFACE OPTIONS NEED TO OPTIMIZE THE TRADE-OFFS AMONG CAPACITY, BANDWIDTH, EFFICIENCY, AND SYSTEM CONSTRAINTS.

Microprocessor-based systems are ideal for executing an essentially infinite number of tasks. The host microprocessors support a limited set of instructions that can combine to produce incredibly complex software programs. In other words, a microprocessor is a piece of hardware designed to be as general-purpose as is feasible, to target as many applications as possible. Moore's Law states that microprocessors will double in complexity roughly every two years. This remarkably accurate prediction has resulted in the latest multicore processors that enable the convergence of cutting-edge technologies.

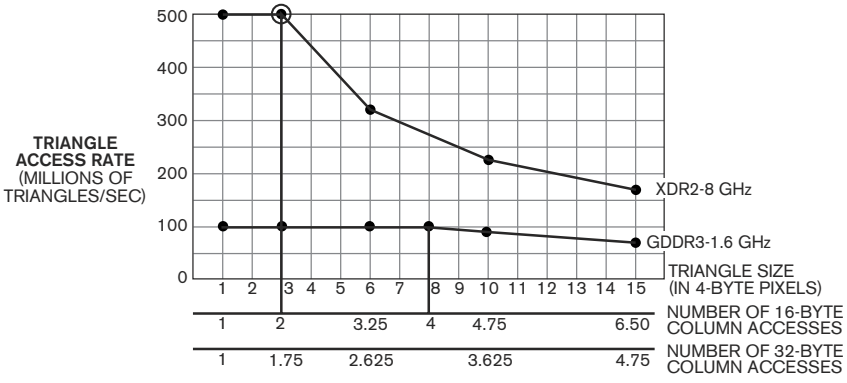

Figure 1 The effective triangle transfer rate compares GDDR3 at 1.6 GHz and XDR2 at 8 GHz.

However, a microprocessor does not make up a complete system. In reality, the supporting components in a system are just as important as the microprocessor itself when determining overall capabilities and performance. Just as microprocessors evolve with time into faster and more efficient devices, supporting components are also evolving to include more complex functions and higher performance interfaces.

PCIe (Peripheral Component Interconnect Express) is quickly becoming the peripheral interconnect of choice, because the slower PCI and AGP (Accelerated Graphics Port) buses place bottlenecks on system performance. For similar reasons, DDR2 (Double Data Rate 2) is slowly taking hold as a general-purpose memory to overcome its slower predecessor, DDR. A system's memory interface can affect performance more than any other system-level interface, and no interface offers more choices and configurations.

At the system level, PCIe interfaces offer configurable options in the form of data rates and lane widths (one, two, four, and, in some cases, eight lanes). In contrast, DDR2 interfaces frequently have widths of 4 to 256 bits and offer a multitude of capacity, data-rate, and core-timing-performance permutations. Add the variety of available memory technologies, and system designers end up with the daunting task of finding an optimal configuration for their systems.

DDR, DDR2, RDRAM (Rambus dynamic-random-access memory), GDDR1/2/3 (graphics DDR1/2/3), and XDR (extreme-data-rate) DRAM are all examples of memory technologies that designers frequently use, and each one has its own set of advantages and drawbacks. To add to this already populous technology space, some memory companies have decided to produce specialty memories that offer superior performance for specially targeted markets. RLDRAM (reduced-latency DRAM) and FCRAM (fast-cycle RAM), for example, are two technologies specifically optimized for network-processor manufacturers that require fast internal DRAM cycle times. XDR2 is a new memory technology from Rambus that incorporates microthreading and offers high efficiency for graphics, networking, and consumer-electronics applications.

Depending on system needs, designers must choose a memory technology and configuration that minimizes the overall system cost and maximizes performance. Typically, designers optimize a memory system for any combination of cost versus capacity, peak bandwidth, efficiency, and system-level restrictions. Although capacity seems straightforward enough, when adding more devices to get more memory, designers must carefully consider how to add the memory devices into the system. For example, adding capacity involves a system-level trade-off, because the added memory devices draw more power.

Enterprise servers and supercomputers are often optimized, at least in part, to contain high-capacity-memory systems. The large and complex programs and data sets that servers and super-

computers often access benefit from more capacity. Users access instructions and data stored in rapid-access areas, such as DRAM subsystems, more quickly than those stored in low-speed, high-latency storage areas, such as hard-disk drives. Therefore, in addition to capacity, these systems are also clearly sensitive to peak bandwidth.

Two ways exist to increase the peak bandwidth of a memory system: increased bus width and increased data rate. The latter involves increasing the rate at which data transfers on each data link, and the former involves increasing the number of data links in the memory system to obtain a higher total aggregate bandwidth. For example, to obtain a total aggregate bandwidth of 12.8 Gbytes/sec, a designer could opt for a 128-bit-wide DDR2 system running at an 800-MHz data rate or a 16-bit-wide XDR system running at a 6.4-GHz data rate.

Most of today's memory technologies provide the capability of achieving high total aggregate data rates, but different applications stress the memory system in different ways. The architectural features of any given memory technology dictate its efficiency for a particular application and its corresponding memory-access requirements. The efficiency of a memory subsystem is defined as the percentage of a system's total aggregate bandwidth that provides useful data to and from the host microprocessor and is the reason memory vendors have added specialty memories to their product portfolios.

ROUTING AREA, CROSSTALK SENSITIVITY, EMI, AND POWER DISTRIBUTION ARE ALL EXAMPLES OF SYSTEM-LEVEL RESTRICTIONS THAT DESIGNERS MUST CONSIDER WHEN SELECTING MEMORY TECHNOLOGY.

RLDRAM, for example, does not have higher capacity or peak-bandwidth specifications than many of the mainstream memory technologies but instead has architectural features that increase its efficiency in certain applications, such as networking. System-level restrictions encompass all of the physical limitations involved with implementing a particular configuration of a given memory technology. Routing area, crosstalk sensitivity, EMI, and power distribution are all examples of system-level restrictions that designers must consider when selecting memory technology.

OPTIMIZING FOR CAPACITY

Although servers and supercomputers clearly benefit from high-capacity-memory systems, designers of these and other products must determine an optimal means to obtain added capacity. Adding devices to memory subsystems such as those in servers or graphics cards is conceptually straightforward regardless of the memory technology. DDR, DDR2, and GDDR devices are capable of multidrop topologies with certain limitations.

Multidrop topologies in a memory system are those in which each link of the data bus connects to more than one DRAM device. For DDR2 systems, you can connect as many as four devices on each data link. Because GDDR-family devices usually have higher peak data rates, signal-integrity issues typically prevent more than two connections per link, and even then only if the devices reside in close proximity, such as back to back on opposite sides of a pc board.

XDR offers a slightly different approach to scaling capacities. Although the address and command bus is a multidrop configuration, it can connect to 36 devices in sequence on a channel. One reason the XDR address channel supports more devices than DDR links is that DDR multidrop connections are usually stub topologies instead of sequential connections. Stubs generate reflections, which degrade signal quality; with sequential connections, you can electrically compensate for the added capacitive loading of each device along the channel, thereby minimizing impedance discontinuities and their resulting reflections.

Each data link in an XDR system, however, is routed point to point; that is, each data link connects to only one port on the DRAM and one port on the host controller. However, XDR DRAM devices are programmable in width; for example, you can program a ×16 DRAM to act like a ×8, ×4, or ×2 device. Low-capacity systems program each DRAM wider, with more links connecting to each device. Adding capacity merely involves programming the devices to be narrower and connecting fewer data links to each device.

A 32-bit XDR interface can support as little as 64 Mbytes and as much as 1 Gbyte of memory. For systems that require high capacities, an emerging technology, FBDIMM (fully buffered DIMM), introduces a buffer IC onto a module packed with many memory devices. The buffer-IC module connects to the host controller through a serial link, thereby saving controller pins and board-routing area. The buffer chip also connects on the module to each DRAM device and acts as an intermediary between host requests and DRAM responses.

Theoretically, a 32-bit interface could connect to 32 multigigabyte modules.

Each of the above technologies provides its own advantages and drawbacks. Engineers widely use the multidrop topology of a DDR system, but it has limited bandwidth scalability due to complex timing and signal-integrity constraints. XDR is scalable and provides an appropriate cost/capability trade-off but is just now entering production volumes. FBDIMM is an architecture not specifically tied to a particular memory technology, and it provides a high-capacity capability. However, the capacity comes with added latency and a significant price tag, especially at this early stage of the technology's life cycle.

OPTIMIZING FOR BANDWIDTH

The need for peak bandwidth drives the memory configuration for many applications. Graphics processors, for example, require constant buffering of rendering and frame data to memory. Games, CAD, and digital-content-creation applications all drive the need for higher peak bandwidth due to complex workloads. 3-D-graphics applications require additional bandwidth to render more realistic scene environments with more polygons, richer textures, and additional postprocessing enhancements, such as antialiasing. The latest high-performance graphics cards use 256-bit GDDR3 memory interfaces with 1-GHz data rates for a total aggregate bandwidth of 32 Gbytes/sec.

However, peak bandwidth is not the only parameter to consider when optimizing for bandwidth. Remember that efficien-


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cy refers to the percentage of a memory system's total aggregate bandwidth that a controller can actually use. Fewer banks and a higher t_{RC} (row-cycle time) in a DRAM device yield more frequent bank conflicts. Bank conflicts drastically reduce the efficiency of a memory system by forcing potentially long periods of inactivity on the data bus. Write-to-read and read-to-write turnarounds also require long periods of inactivity on the data bus.

Memory systems can experience reduced efficiency even with the data bus active 100% of the time. To keep internal pipelines full, DRAM devices implement a feature called prefetch, which allows the DRAM core to run slower than the DRAM interface. The prefetch of a DRAM technology essentially determines how much data transfers for any given transaction, commonly referred to as access granularity.

In the above example, GDDR3 implements a prefetch of four, and a single transaction would therefore yield 32 bytes of data in a configuration that allows for fine access granularity. Graphics processors work largely with units called triangles, and, as graphics-processor generations mature, each triangle decreases in bytes, because smaller triangles yield more realistic rendered images. A transfer of 32 bytes may be more than necessary to access the triangles needed for a process. For example, if only one 4-byte triangle were necessary from memory, 28 bytes of the corresponding access would go to waste. Even though the bus is active during the entire transfer, the efficiency of the transfer significantly reduces. New memory technologies, such as XDR2, are emerging to further enhance bandwidth efficiency for various applications. **Figure 1** shows the effective triangle transfer rate versus triangle size for GDDR3 at 1.6 GHz and XDR2 at 8 GHz. Designers optimizing their memory system for bandwidth must consider both peak bandwidth and efficiency to get the best performance out of their host processor.

MICROPROCESSORS TARGETING SPECIFIC APPLICATIONS MAY GAIN PERFORMANCE FROM THEIR MEMORY SYSTEMS BY INTEGRATING THE MEMORY INTERFACE DIRECTLY ONTO THE PROCESSOR ITSELF.

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OPTIMIZING FOR SYSTEM CONSTRAINTS

Architectural factors, such as capacity and bandwidth, don't limit many designers; however, these designers must still consider total system cost and physical limitations when configuring the memory system. DRAM devices often make up the most expensive portion of a system's BOM (bill of materials), and designers should make every effort to use the fewest devices possible to meet the architectural goals. Expanding on the example above, one XDR device or eight DDR2 devices could satisfy a microprocessor that demands 64 Mbytes of memory with 12.8 Gbytes/sec of total aggregate bandwidth. If the same microprocessor were to demand the same bandwidth but with 1024 Mbytes of memory, eight 1-Gbit DDR2 devices could still satisfy the requirement; however, achieving the same capacity with XDR would require 16 512-Mbit devices until 1-Gbit devices enter mass production.

If the product were particularly sensitive to total system cost, then an option enabling the lowest memory-system BOM cost for the particular system requirement would be ideal. In addition, as data-link speeds increase, signal-integrity concerns, such as EMI, crosstalk, reflections, and power-supply noise, become much more important. Aside from the usual system optimizations, such as stub-length reduction, trace shielding, and supply bypassing, the memory configuration itself can play a role in easing signal-integrity issues. Single-ended traces typically require less room to route on a pc board, but differential data links provide more immunity to crosstalk and EMI radiation.

Low-voltage swings reduce the stress on I/O power supplies as do differential drivers, which drastically reduce di/dt noise. Slower memory technologies are generally easier to route on a pc board, given the eased timing-skew restrictions. Designers must take care with high-speed-memory designs to ensure minimal flight-time skew between data links. Strobe-based systems, for example, introduce complex timing constraints at both the silicon and pc-board levels. New technologies, such as FlexPhase, dynamically calibrate out skew in the datapath but are not integrated into all available memory-interface cells on the market. DDR2, GDDR, and XDR all use on-die termination that minimizes stub reflections, but multidrop DDR2 and GDDR topologies still have stubs between devices. In addition to architectural parameters, designers should consider system constraints when choosing a memory configuration.

Microprocessors are generic devices that you may use for specific applications. Decoupling the memory interface from the microprocessor keeps the processor more generic in scope and enables multiple designs to use different memory configurations with the same processor. On the other hand, microprocessors targeting specific applications may gain performance from their memory systems by integrating the memory interface directly onto the processor itself.

Regardless of the application, designers have many choices when specifying the memory subsystem and should take care to optimize the trade-offs among capacity, bandwidth, efficiency, and system constraints. Most of today's memory technologies ensure that virtually any application has a sufficient if not optimal memory-system technology. Whether it's XDR for high-performance and low-cost optimization or DDR2 for high-capacity commodity systems, system designers and chip architects have a full menu of options that can save money and boost performance. EDN

AUTHOR'S BIOGRAPHY

Victor Echevarria is a product-marketing manager in the Platform Solution Group at Rambus Inc. He currently manages product-marketing activity for the RDRAM and XDR product lines for new and existing customers. Echevarria joined Rambus in 2002 as a systems engineer. Before joining Rambus, he worked with Agilent Technologies, where he developed software for its high-speed digital-sampling oscilloscopes. Echevarria graduated from the University of California—Berkeley, in 2002 with a BS in electrical engineering and computer science.

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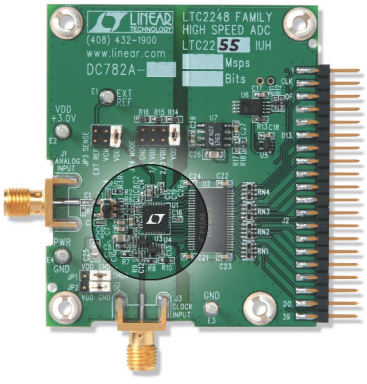

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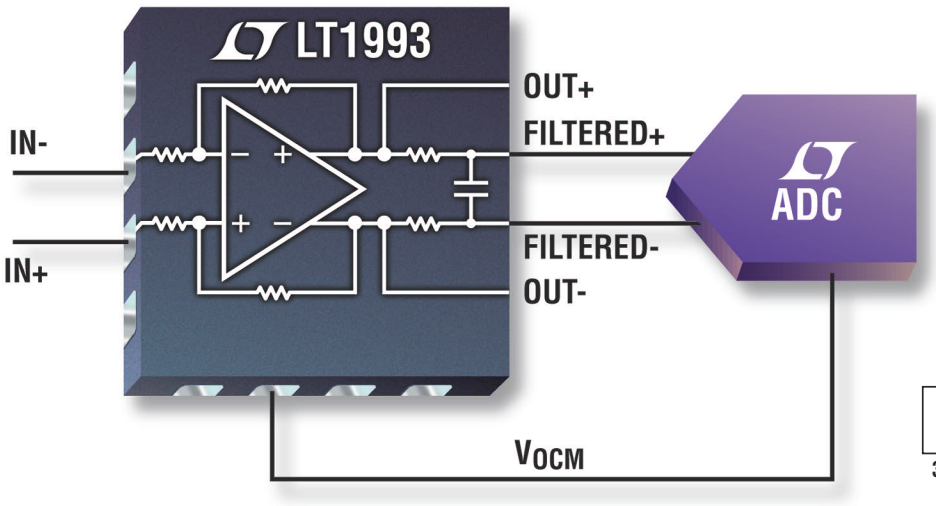

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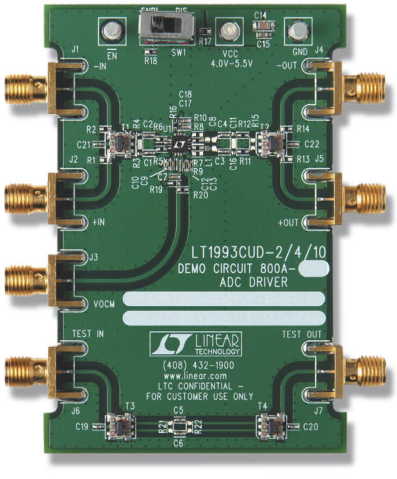

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DIs Inside

When processing signals from analog sensors, you frequently encounter wide variations in attenuation among communication channels or sensors. Or, you face situations in which several identical sensors within a supervised system return signals of roughly similar spectral composition and dynamic range but with considerably different maximum amplitudes. Sometimes, it's possible to predict these and other variations and adjust the gain of preprocessing amplifiers. More frequently, you encounter unpredictable signals and thus lose data associated with nonrepeatable events. In these circumstances, an adaptive preamplifier with AGC (automatic gain control) can prevent measurement-channel saturation and data loss.

AGC preprocessing suppresses the absolute amplitude of a sensed signal while preserving the best possible resolution of individual spectral components' relative amplitudes. The circuit in this Design Idea offers one relatively simple and efficient approach to per-channel AGC. The circuit uses a method of direct low-level signal control using a short-circuited bipolar transistor. In **Figure 1**, a variable voltage divider comprising a fixed resistance, R_1, and a variable resistance controls the signal's ac amplitude. The variable resistance comprises the differential resistance of a bipolar transistor, Q_1, short-circuited from base to collector. To vary Q_1's resistance, you force direct current into the shorted transistor from a current source comprising voltage source V_{REG} and a high-value resistor, R_2. To prevent R_2 from affecting the circuit's ac-voltage-transfer characteristic, R_2's resistance must greatly exceed R_1's.

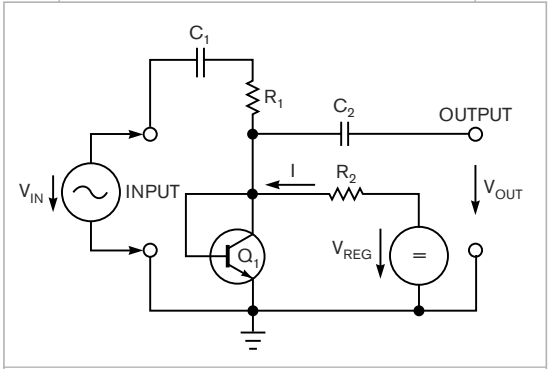

Figure 1 A short-circuited bipolar transistor forms one element of a basic attenuator circuit.

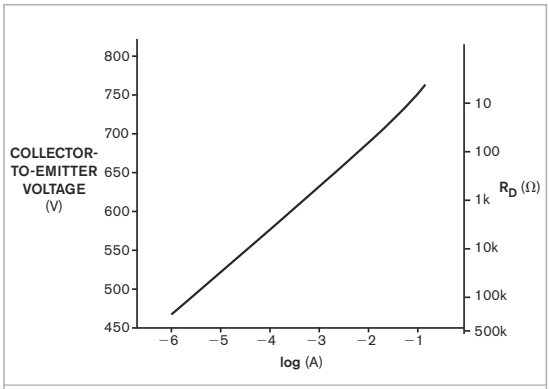

Figure 2 A VI characteristic shows the corresponding differential-resistance graph for a short-circuited BC337-16 transistor. (Note: The -16 denotes a sorted h_{FE} range of $100<h_{FE}<250$.)

For all reasonable values of positive current I—generally, less than the transistor's maximum rated emitter current (I_E)—transistor Q_1's collector-to-emitter saturation voltage is less than its base-emitter threshold voltage, and the transistor operates in the active state. The shorted transistor's VI (voltage-versus-current) characteristic curve strongly resembles that of a PN diode and follows Shockley's Equation except for slightly higher dc-voltage values. That is, the device's voltage variation is proportional to the logarithm of the dc-current variation.

Therefore, the shorted transistor's differential resistance at every dc operating point along the VI curve is inversely proportional to the passing dc current; in other words, the device's differential conductance is directly proportional to the current. Because, in its active state, a common-emitter-connected bipolar transistor's current-amplification factor is typically 100 or more, the differential resistance accurately follows this rule over a broad range of currents.

Thus, varying V_{REG} in **Figure 1** varies the current, I, and controls the R_1-Q_1 voltage-division ratio. Coupling capacitors C_1 and C_2 separate the

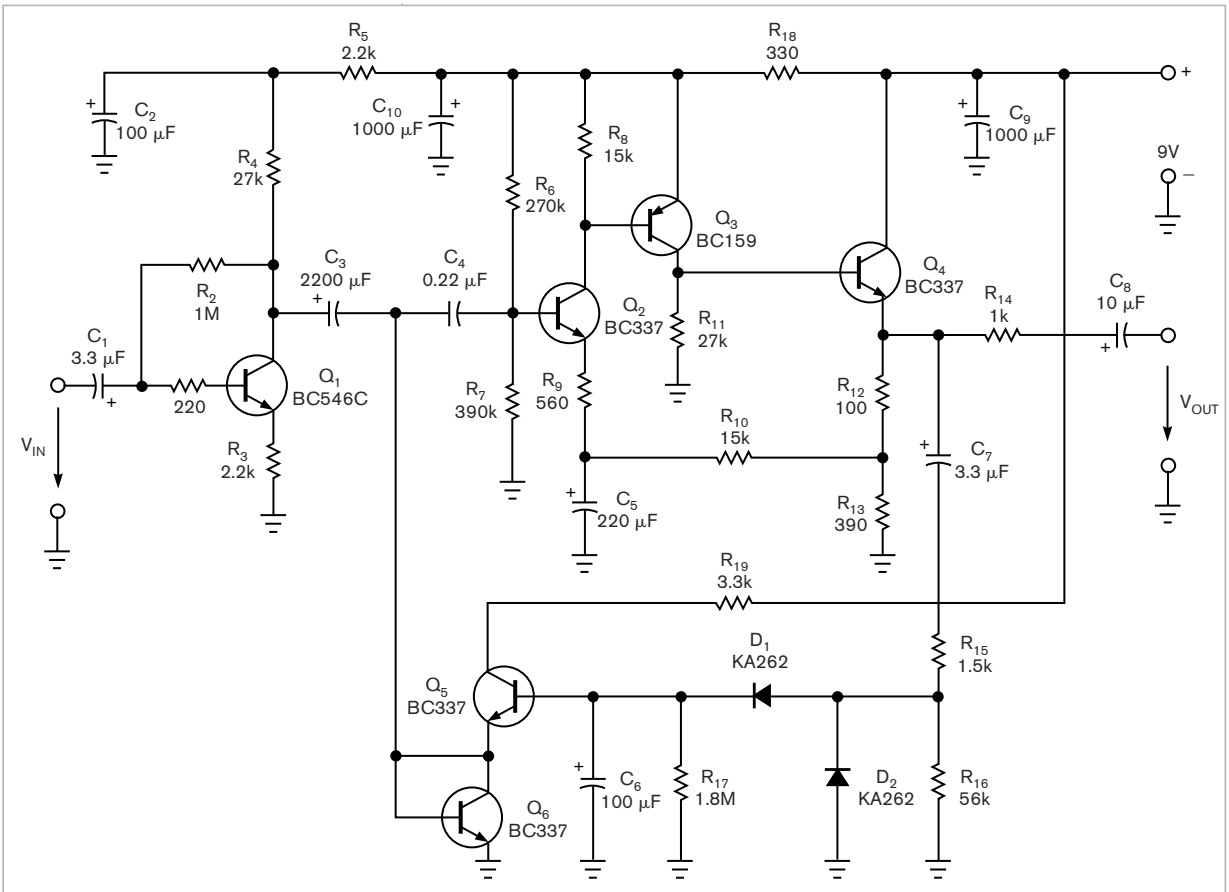

Figure 3 You can assemble this AGC circuit entirely from discrete components.

circuit's attenuator from the input-signal source and output load. **Figure 2** illustrates a typical small-signal bipolar transistor's short-circuited VI characteristic, showing that you can control differential resistance over at least five decades of range—that is, more than 100 dB.

In a practical circuit, the finite values of R_1 and R_2 limit the control range. For proper operation and to keep the signal's THD (total-harmonic-distortion) factor, k, below 5%, the output-voltage amplitude, V_{OUT}, should be just a few millivolts. Even with these limitations, this attenuator circuit appears to offer one of the best and simplest AGC circuits.

Figure 3 shows the completed circuit design. The input signal, V_{IN}, drives buffer stage Q_1, whose unbypassed emitter resistor, R_3, serves four purposes. First, it increases Q_1's differential output resistance to the approximate value shown in **Equation 1**:

$$R_{D1} \approx \frac{h_{11E} + h_{21E}R_3}{h_{11E}h_{22E}}. \quad (1)$$

The increase in the circuit's differential output resistance is so large that the value of R_4, 27 kΩ, almost exclusively determines the overall output resistance. Second, leaving R_3 unbypassed reduces Q_1's voltage gain to:

$$A_{IC1} = \left(h_{22E}R_3 - h_{21E}\right)R_4 / \left(R_3 + R_4\right)D_{hE} + \left[h_{21E} + 1 - h_{12E} + \left(R_3 + R_4\right)\right] R_3 + h_{11E} \approx -R_4 / R_3. \quad (2)$$

This **equation** simplifies to $A_{IC1} \approx R_4/R_3$. (Note that D_{hE} denotes the determinant $(h_{11E} \times h_{22E} - h_{12E} \times h_{21E})$, which this Design Idea includes for theoretical accuracy. However, you can neglect the numerical value of D_{hE} for modern silicon transistors without significantly affecting the calculation's accuracy.) Third, as **Equation 2** shows, leaving R_3 unbypassed helps linearize the response of Q_1's collector current-to-voltage drive. Fourth, Q_1's differential base input resistance rises to: $R_{dBASE} = h_{11E} + h_{21E} \times R_3$, which is larger and less dependent on Q_1's instantaneous operating point than h_{11E} alone.

In **Figure 3**, resistor R_4 forms the variable attenuator's fixed resistance, analogous to the upper resistor, R_1, in **Figure 1**, and Q_6 forms the attenuator's variable-resistance element. Transistor Q_5 supplies Q_6's collector-drive current, and Q_5's common-emitter configura-

(continued on pg 92)

LINEAR TECHNOLOGY

DESIGN NOTES

"Easy Drive" Delta-Sigma Analog-to-Digital Converters Cancel Input Current Errors – Design Note 368

Mike Mayes

Introduction

It is now possible to place large RC networks directly in front of high resolution ΔΣ analog-to-digital converters without degrading their DC accuracy (see Figure 1). The LTC®248x family of converters solves this problem with Easy Drive™ technology, a fully passive sampling network that automatically cancels the differential input current. Easy Drive technology does not use on-chip buffers, which compromise performance (see What is Wrong with On-Chip Buffers?), but instead uses a new architecture that maintains 0.002% full-scale error with input RC networks up to 100kΩ and 10μF. This new technology offers many advantages over previous generation ΔΣ ADCs:

- Rail-to-rail common mode input range
- Direct digitization of high impedance sensors
- Elimination of sampling spikes seen at the ADC input pins
- Simple external lowpass filtering
- Noise/power reduction
- Cancellation of external RC settling errors
- Easy interface to external amplifiers
- Removal of transmission line effects for remote sensors

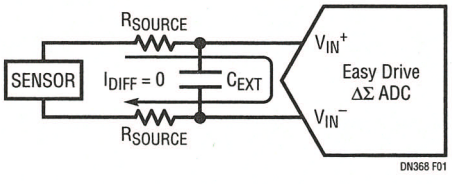

Figure 1. Easy Drive Technology Automatically Cancels Differential Input Current, Thus Allowing Direct Digitization of Large External RC Networks

How Does it Work?

Delta-Sigma converters achieve high resolution by combining many low resolution conversions into one high resolution result. Most commercially available ΔΣ converters combine hundreds or even thousands of 1-bit conversions into a single 16-, 20- or 24-bit result. The obvious advantage is that it's much easier to implement a 1-bit converter than a 24-bit converter. In order to achieve high resolution, the input is sampled many times during the conversion cycle.

The problem is that the input structure of ΔΣ converters is a switched capacitor network. Capacitors are rapidly switched (up to 10MHz) between the input, reference and ground as a function of the final output code. Each time these capacitors are switched to the ADC input, a current pulse is generated. A pattern of charging/discharging pulses is seen at the input pin of the ADC. This pattern is a complex function of the input and reference voltages. External RC networks that do not completely settle during each sample period cause large DC errors.

The trick to solving this problem is to take advantage of the oversampling properties of ΔΣ converters. The front-end capacitor switching on a per sample basis is identical to conventional ΔΣ converter sampling. An innovative front-end sampling architecture controls the switching pattern of the capacitor array. When summed over the entire conversion cycle, the total differential input current is zero, independent of the differential input voltage, common mode input voltage, reference voltage or output code. The common mode input current is constant and proportional to the difference between the input common mode voltage and reference common mode voltage.

RC networks placed in front of ΔΣ ADCs significantly improve their performance and ease-of-use while providing lowpass and antialias filtering. External RC networks applied to the input of the LTC248x simply integrate (average) the input current spikes generated by the ADC. Since the average differential input current is zero, the total error introduced by the external RC network is zero if the resistance tied to the plus/minus inputs of the ADC is balanced. Resistances up to 100k, combined with

capacitors up to 10µF may be placed in front of the ADC with less then 0.002% full-scale error (20ppm), while conventional ΔΣ ADCs with the same input network have greater than 10% full-scale errors (100,000ppm). Furthermore, no errors are introduced even if the external resistances are not balanced, as long as the common mode input voltage is equal to the common mode reference voltage. Even if the common mode input voltage does not match the common mode reference voltage, the differential input current remains zero and the common mode input current results in an offset voltage which may be removed through system calibration.

Direct digitization of external sensors with impedances up to 100kΩ is now possible without the need for external or on-chip amplifiers (see Figure 2). Bridges, RTDs, thermocouples and other sensors may tie directly to the ADC input. The addition of external capacitors reduces the charge kickback spikes seen at the input of the ADC. An external 1µF capacitor reduces a 1V spike to 18µV. This improves the noise performance of systems where the sensor cannot be placed near the ADC input and eases the drive requirements in applications where external amplifiers are used. The addition of a large resistor between the amplifier output and the ADC input isolates the amplifier from the large bypass capacitor, thus improving its stability.

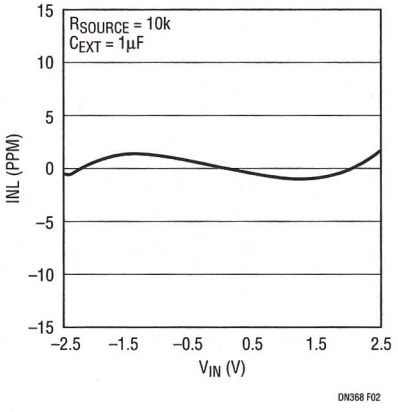

Figure 2. Easy Drive Technology Directly Digitizes Large External RC Networks Without Degrading Linearity

What is Wrong with On-Chip Buffers?

One historical solution to the input current settling problem is to integrate a buffer amplifier on the same chip as the ΔΣ ADC. This isolates the ADC input from the switched capacitor array making the ADC input appear high impedance. While this solution looks good on paper, the fact is data converters using on-chip buffers suffer from the limitations of those amplifiers. The common mode input range can no longer swing rail-to-rail. Input signals need to be shifted at least 50mV above ground and a volt or more below V_{CC}. Amplifier offset errors, offset drift, PSRR, CMRR and noise are combined directly with the input signal and result in reduced converter performance. Additionally, on-chip amplifiers require significant power in order to drive the high speed capacitive sampling network. For these reasons, most manufacturers of ΔΣ ADCs using this technology offer a mode to shut off and bypass on-chip amplifiers.

Another solution is coarse/fine input sampling. During the first half of the sampling period (coarse), the input voltage is sampled through an on-chip buffer amplifier, thus isolating the ADC input from the charging capacitor. During the second half of the sampling period (fine), the buffer is switched off and the capacitor is tied directly to the input. While this decreases the magnitude of the spikes seen at the input of the ADC, it results in nonlinear settling errors as a function of op amp offset voltage, CMRR, input signal level and external RC time constants. For these reasons, manufacturer's of ΔΣ ADCs using this technology bypass course/fine sampling for input signal levels below 100mV.

Conclusion

New Easy Drive technology simplifies the drive requirements of ΔΣ ADCs. The solution lies in a purely passive input current cancellation algorithm that enables rail-to-rail inputs without the added power requirements of on-chip buffer amplifiers and the errors they introduce. Easy Drive technology enables ΔΣ ADCs to directly interface to high impedance sensors, lowpass filters and input bypass capacitors without degrading the DC performance.

Devices using the Easy Drive technology are currently available in 16- and 24-bit versions with an on-chip temperature sensor, no latency conversions for simple multiplexing, on-chip oscillators with guaranteed line frequency rejection, precise DC specifications and the ease-of-use common to all of Linear's ΔΣ ADC converters.

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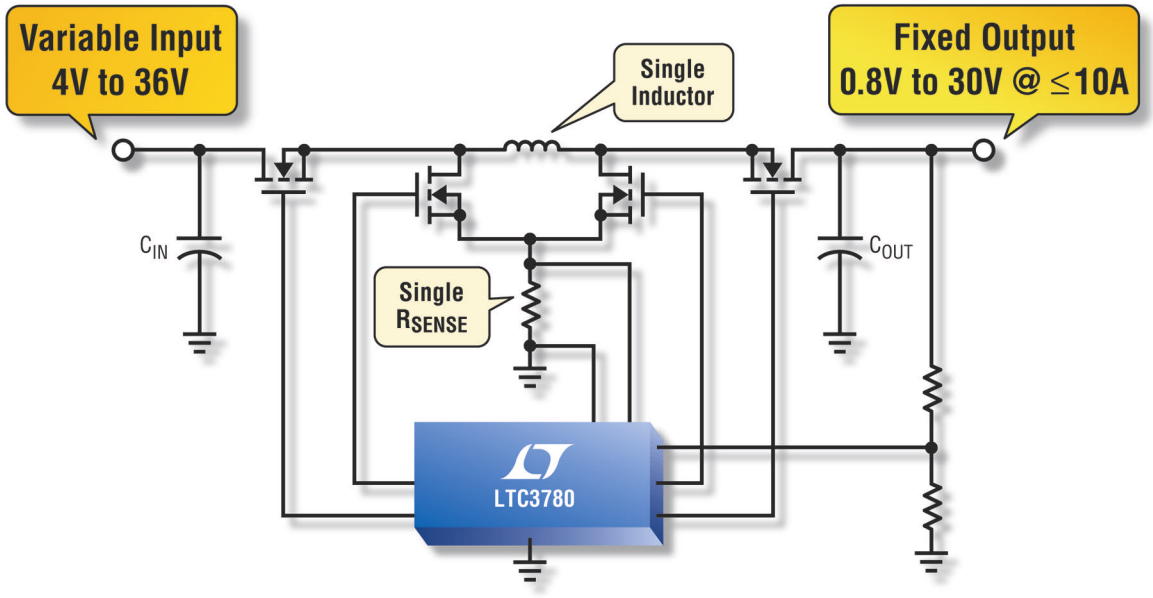

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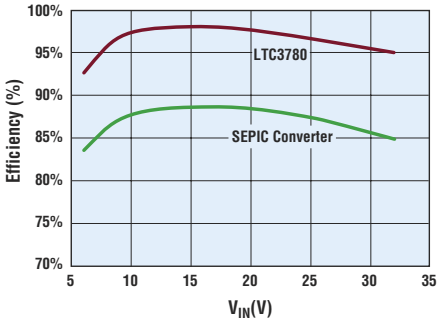

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tion draws little base current. This approach enables use of a high value for AGC-release time-determining resistor R_{17}, thus permitting a long AGC-release time. Resistor R_{19} limits the maximum dc control current through Q_5 and Q_6.

The large value of C_3, when you compare it with Q_6's minimum differential resistance—that is, its maximum signal amplitude—at full control, presents negligible reactance to the lowest frequency-signal-spectrum component. A voltage-doubler rectifier comprising D_1 and D_2 extracts a portion of the signal from output stage Q_4 and produces the control voltage for Q_5. This arrangement accommodates both polarities of large peak amplitudes of nonsymmetrical signal waveforms. Resistor R_{15} determines the AGC's "attack" time. Too small values of R_{15} in combination with C_6 can lead to instability by creating a pole in the feedback-transfer function. Resistor R_{17} determines the AGC-release time.

To secure good response to high-frequency-signal components, use either Schottky or fast PN silicon diodes for D_1 and D_2. The dc-coupled complementary cascade comprising Q_2 and Q_3 supplies most of the circuit's voltage gain. A 1-kΩ resistor, R_{14}, isolates Q_4, the output-emitter follower, from the signal-output terminal. If necessary, you can use a lower resistance at R_{14}, but a large-capacitance connecting cable can provoke Q_4 into parasitic oscillation if R_{14} is too low.

Figure 4 shows the circuit's input-versus-output characteristics as measured with a sine-wave signal. The effective AGC range extends from 100-μV- to 100-mV-rms input voltage, a 60-dB dynamic range. Output voltage varies less than 2 dB over this input range, reaching a nominal level of 775 mV rms at a −20-dB- (100-μV-rms) input level. The input's 0-dB point is set arbitrarily at 1-mV-rms input, which corresponds to an 803-mV-rms output. The AGC attack time for a sinusoidal-input-signal step from 0 to 100 mV rms is approximately 0.3 sec, and the AGC release from 100-mV-rms input to −20 dB (100 μV rms) is approximately 100 sec. **Figure 4** also includes a graph of THD versus input voltage. The distortion is well below a 5% THD limit throughout the input-voltage range.

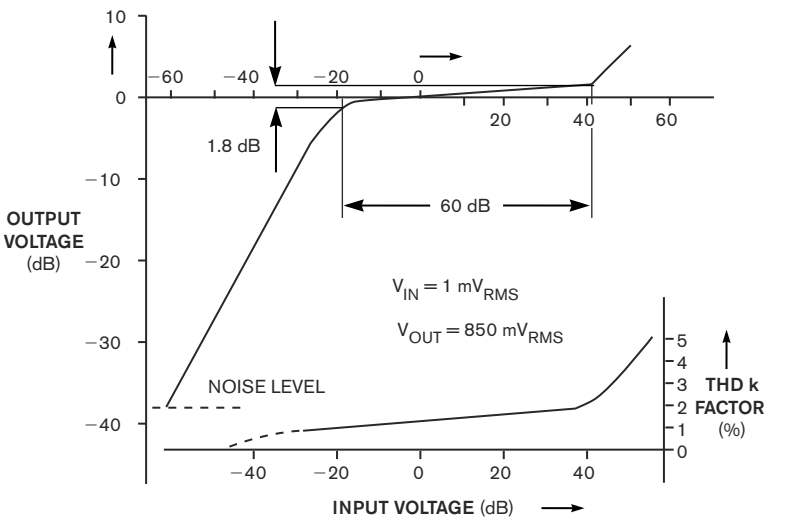

Figure 4 The circuit's input-versus-output characteristic shows a 60-dB control range (upper trace) and total harmonic distortion well below 5% over the control range (lower trace).

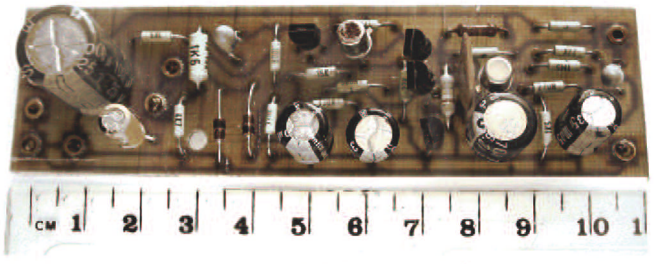

Figure 5 A single-sided pc board accommodates the assembled AGC amplifier.

To measure the attenuator's baseline input noise, terminate the input with its nominal 1-kΩ source resistance. At low input voltages, input stage Q_1's noise limits the processed signal's usable dynamic range. The rms noise level is about −38 dB relative to the nominal output for input signals below the AGC threshold. When the AGC becomes active, the SNR increases in proportion to the AGC reduction. For example, with a 0-dB- (1-mV-rms) input signal, the SNR increases to approximately 60-to-1.

If you assemble the circuit using the passive-component values in **Figure 3**, the amplifier's −3-dB bandwidth spans 45 Hz to 35 kHz. At a power-supply voltage of 9V, no-signal current consumption is approximately 12 mA. **Figure 5** shows a photograph of the assembled pc board. EDN

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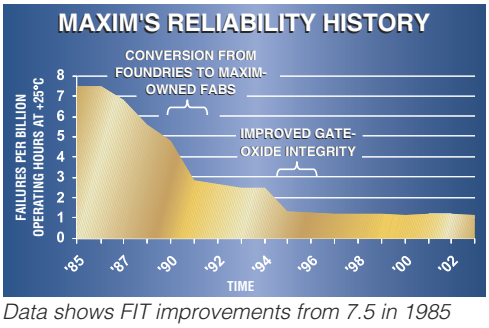

Data shows FIT improvements from 7.5 in 1985 to 1.13 in 2003.

Photo courtesy NASA/JPL-Caltech.
*The Cassini spacecraft uses Maxim's high-speed ADC.

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Precision active load operates as low as 2V

By Joel Setton, Crolles, France

This Design Idea presents a self-powered, precision-active-load circuit that improves on a previously published design (**Reference 1**). Added features include a wider operating-voltage range of 2 to 50V or higher and several flexible current-setting modes. The circuit in **Figure 1** uses National Semiconductor's LM10, which suits this application. The LM10's reference section, IC_{1A}, generates a precision 1.2V reference voltage, V_S. Resistive divider R_1 and R_2 applies a fraction of V_S to IC_{1A}'s reference amplifier, which drives shunt regulator Q_1.

Transistor Q_3 acts as a current mirror of transistor Q_2's collector current and supplies power to shunt regulator Q_1. Resistors R_9 and R_7 set the current-mirror ratio, and the current through resistor R_9 depends on the current through R_6, which V_S establishes. As a result, Q_3, which mirrors the collector current of Q_2, provides power to the shunt regulator. V_S sets R_6, which determines the current through R_9. Thus, the LM10's reference section regulates both its own power-supply voltage and the current that Q_3 provides.

At power-on, Q_2, Q_3, and Q_4 are all off. Resistor R_{10} draws a small amount of start-up current, which Q_3 amplifies to start the current-mirror process. When sufficient current flows through R_7, Q_4 saturates, and R_9 and R_7 then set the current-mirror ratio. The active load's power-handling section comprises the LM10's operational-amplifier section, IC_{1B}, and power transistors Q_6 and Q_8. A 10-turn precision potentiometer, P_1, and range-selection switch, S_1, set the load current as follows:

On Range A, the load current varies at 1A per turn of P_1—that is, 10A maximum with P_1 set fully clockwise. On Range B, the load current varies at 100 mA per turn of P_1—that is, 1A maximum with P_1 set fully clockwise. On Range C, an external voltage source that connects to R_{13} controls the load current at a rate of 1A per volt with P_1 set fully clockwise. You can drive the external input with a function generator to test a power supply's transient response. On Range D, the load circuit emulates an adjustable power resistor with load current proportional to the voltage across the load's terminals. The equivalent resistance varies with P_1's setting—that is, $R_{LOAD}=100\Omega/N_{TURNS}$. Range E is similar to D, with a resistance of $10\Omega/N_{TURNS}$.

To calibrate the circuit, connect it to a suitable power supply delivering any voltage from 2 to 50V. First, set P_1 to one turn—that is, one-tenth of full-scale—and S_1 to Range B. Adjust R_{17} for a 100-mA output current. Then, rotate P_1 fully clockwise and adjust R_{20} to set the output current to 1A. Repeat these two adjustments in sequence because they interact slightly. Current that IC_1 draws through Q_3 sets the minimum current through the load circuit at slightly less than 1 mA.

Because the circuit operates at 2 to 50V, it is suitable for testing the low-voltage outputs of a PC's power supply. You can extend the maximum voltage by selecting suitable transistors for Q_2, Q_3, and Q_5 through Q_8; the LM10's regulated power-supply voltage does not link to the external voltage. Note that when dissipating large amounts of power, transistors Q_6 and Q_8 require adequate cooling to maintain safe junction temperatures. EDN

REFERENCE

1 Toffoli, Tommaso, "Self-powered dummy load checks out multiple power supplies," *Electronic Design*, April 17, 2000, pg 118.

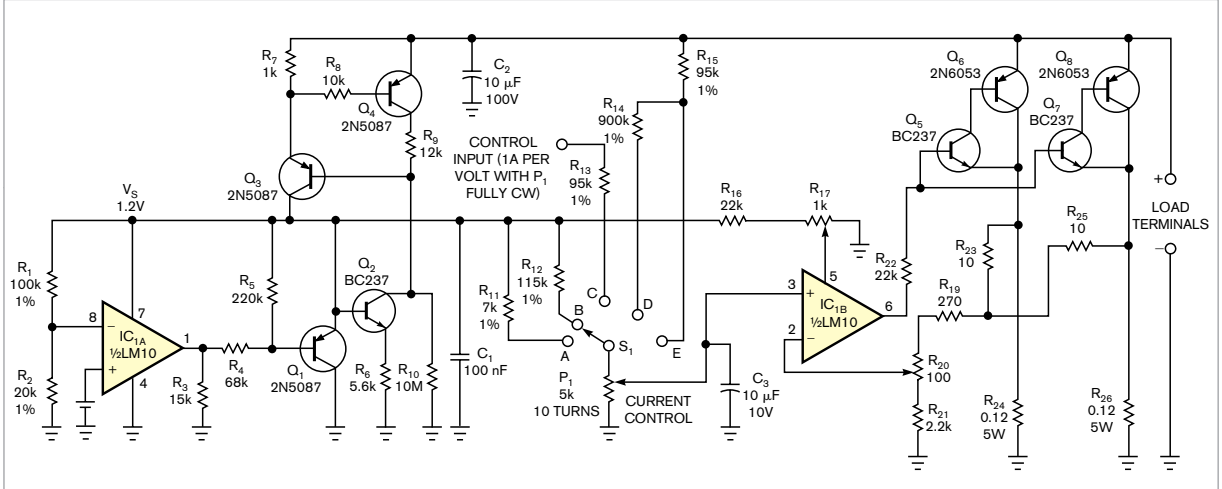

Figure 1 This versatile precision load circuit draws constant current or emulates an adjustable power resistor.

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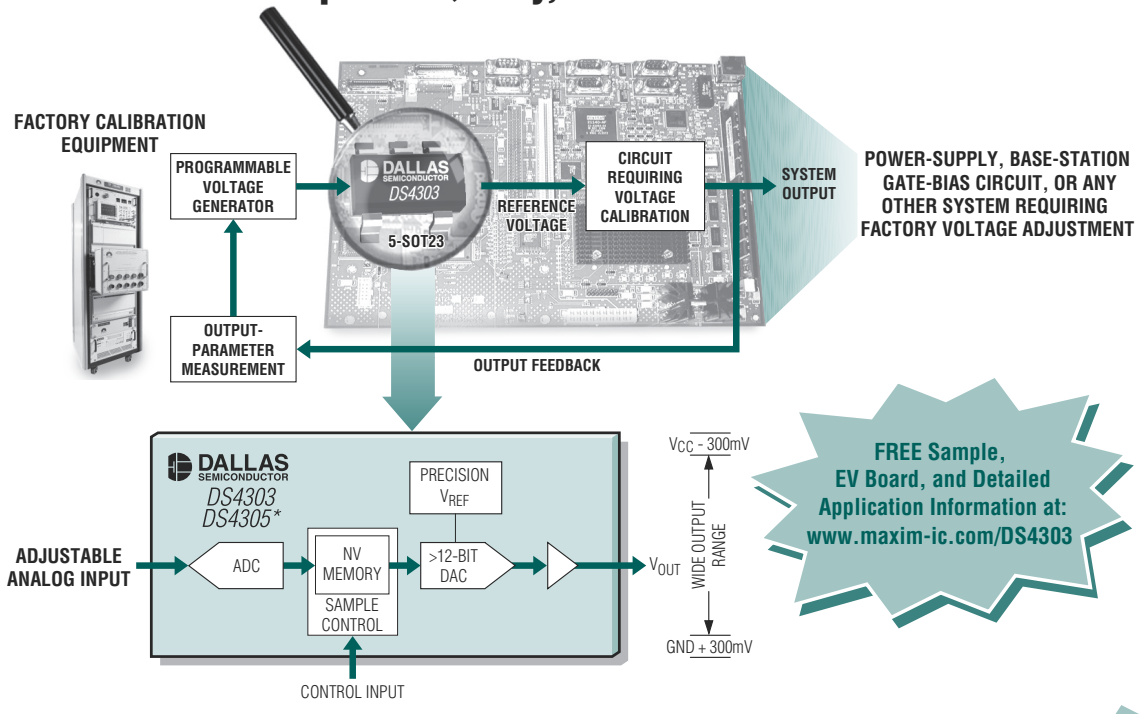

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Squeeze extra outputs from a pin-limited microcontroller

Abel Raynus, Armatron International Inc, Malden, MA

Many of today's designs use low-cost microcontrollers from Freescale and Microchip, but during the last decade, device packages have resorted to ever-smaller footprints featuring as few as eight or even six pins. Although these packages minimize pc-board area, they also reduce the number of available I/O pins and pose problems for designers who need to add one more function without migrating to a device that occupies a larger package.

To overcome a shortage of inputs, a designer can increase a small microcontroller's inputs by writing a program that multiplexes and polls the input pins. However, this approach doesn't lend itself to extending outputs, because most designs require simultaneously driving multiple pins. **Figure 1** shows how to solve the problem by adding a shift register.

For example, you can add an eight-LED bar graph to a design based on IC_1, Freescale Semiconductor's 9-bit, flash-memory MC68HC908QT1 microcontroller, which has only eight pins. The device includes only four general-purpose outputs and thus by default cannot drive eight discrete LEDs. To solve the problem, you can add IC_2, a 74HC595 serial-input/serial-output/parallel-output latching shift register available from On Semiconductor and other vendors. The register's latching function allows selective drive of only those LEDs associated with specific data bits.

According to its data sheet, the 74HC595 accepts signals through the SPI protocol. Unfortunately, low-end microcontrollers, such as the MC68HC908QT1, lack SPI hardware, but you can simulate the SPI in software by following these steps:

1. Unlatch the shift register's outputs by deasserting microprocessor IC_1's PA4 pin.
2. Starting with the MSB, copy a bit from the processor's internal data register and transfer the bit to the processor's PA0 (SD) output.
3. Generate a clock pulse at Pin PA1.
4. Repeat steps 2 and 3 for all eight data bits.
5. Assert the microprocessor's PA4 output to latch the data into IC_2, the 74HC595.

Figure 2 shows the timing diagram for transmitting data byte $F0 from IC_1 to IC_2.

Available from the online version of this Design Idea at www.edn.com/050804di1, **Listing 1** illuminates the LEDs by sending five consecutive bytes to IC_2 and the LEDs: $03, $0c, $30, $c0, and $55. The first four bytes progressively illuminate two LEDs along the bar-graph display at one step per second. The last byte illuminates and latches all odd-numbered LEDs. The **listing** contains only commonly used instructions that easily translate into other microcontrollers' assembly languages.

The SPI requires only three output pins, which frees the microcontroller's remaining I/O pins for other functions and allows remote installation of the shift register/LED driver—for example, on a separate display board with the LEDs. Also, when suitably buffered, the register's outputs can drive other loads, such as motors, relays, and incandescent lamps. EDN

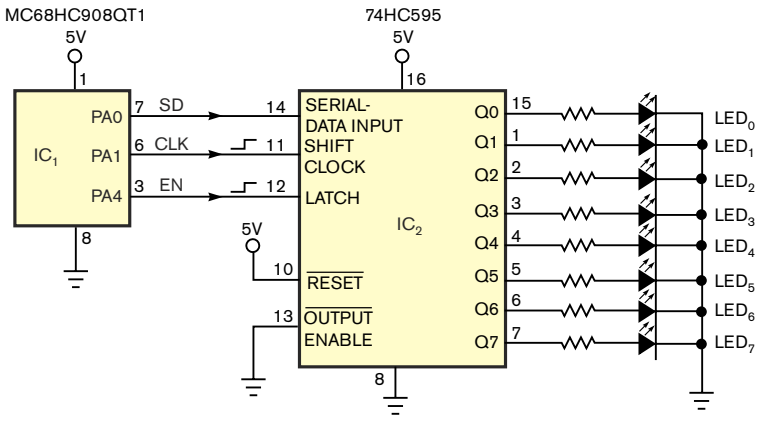

Figure 1 Do you need more outputs? You can emulate an SPI in software to add a shift register to a pin-limited microcontroller.

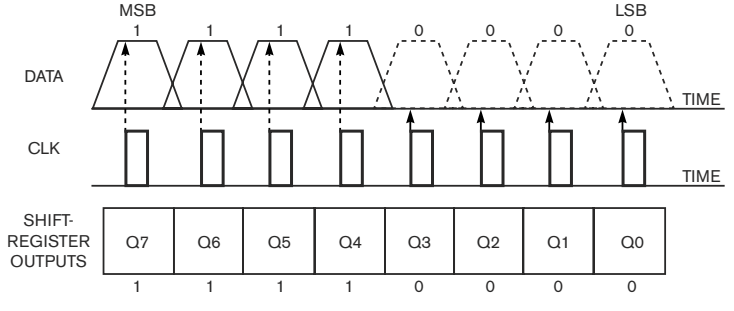

Figure 2 The sample timing diagram illustrates the loading of $F0 byte into an external shift register.

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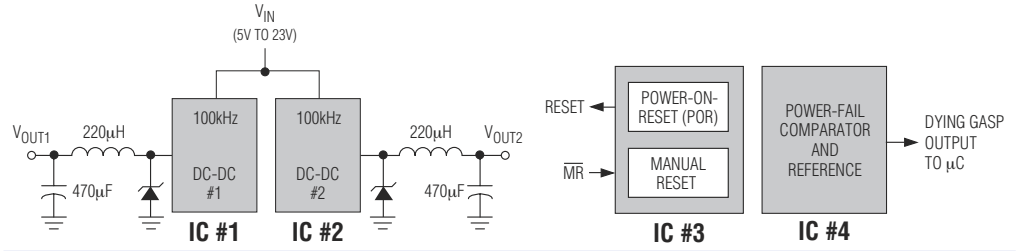

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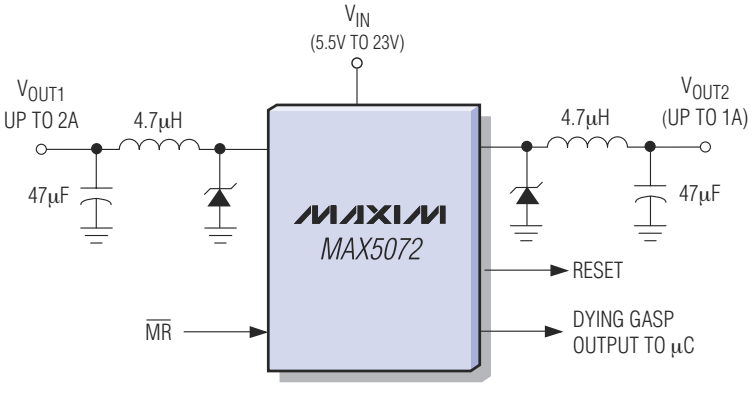

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Aitech, www.aitech.com

Multicolored enclosures allow color matching for corporate identity

Teknet handheld enclosures have elastomer edge grips available in multiple colors and suit in-field test-and-measurement instruments, medical devices, and data-logger applications. The devices measure 6.1×3.78 in. with 0.79-, 0.95-, and 1.11-in. heights with recessed top areas for a membrane keypad. Two models include a battery compartment accepting 1.5V AA cells or one 9V cell, screw pillars in the top and base moldings for fitting pc boards, and assembly by four self-tapping screws. The enclosures cost $14 each.

Teko, www.tekoenclosures.com

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Targeting WirelessUSB (Juno-USB), flash drives, and Wi-Fi applications, this ultrathin enclosure weighs less than 8g and measures 1.8×0.8×0.425 in. Peripherals include a slip-fit protective cap and binding button, internal features that enable pc-board mounting, and a press-together fit for reduced assembly time and setup costs. Available in a variety of colors, the cover accepts artwork, overlays, and printing. With endless CNC modifications available, the enclosure costs 78 cents (250 to 500).

New Age Enclosures, www.newage enclosures.com

productroundup

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Bud Industries Inc, www.budind.com

Thermal-interface material comes in various shapes and sizes

Targeting high-volume automatic-dispensing and -placement applications, the SIL-PAD 1500ST (soft track) high-performance, fiberglass-reinforced, silicone-based thermal interface has a thermal impedance of 0.23°C-in.^{2}/W at 50 psi and an inherent tack on both sides of the material. The inherent tack eliminates the need for additional adhesive layers, which decrease thermal performance by increasing interfacial resistance. The material comes in sheet form; bulk roll; and full die-, kiss-, or butt-cut parts. The 1×1×0.008-in. product costs 51.8 cents (5000).

Bergquist Co, www.bergquistcompany.com

Cabinet cooler has no moving parts

Vortex tubes allows this 2800-BTU/hour cabinet cooler to cool compressed air to 20°F. The cooler mounts to NEMA 12, 4, or 4× stainless-steel enclosures through an electrical knockout. With no moving parts to wear out, the device suits large electrical enclosures with high heat loads. The cabinet cooler costs $277.

Exair Corp, www.exair.com

Floating-point library has more than 100 functions and transforms

The GDD600 library of floating-point DSP vectors and functions features a data-conversion unit that facilitates the conversion of fixed-point and integer formats into floating-point units and converts floating-point units into integer form. With more than 100 functions and transforms, the library performs operations including fast-Fourier transforms, fast-Hartley transforms, discrete-cosine transforms, FIR/IIR filters, coordinate transforms, vector operations, complex-number arithmetic operations, pseudorandom-number generation, and data-conditioning operations. The GDD-600 suits Texas Instruments TMS320 DSP-based platforms and costs $5500.

Sundance Digital Processing Inc, www.sundance.com

DSP offers better performance

The TMS320C6418 DSP has an extended-case-temperature range of −40 to +105°C, 512 kbytes of L2 cache, and an integrated Viterbi co-processor. The peripherals include two McBSPs (multichannel-buffered serial ports), two audio serial ports, a host-port interface, two I^2C control serial ports, and an oscillator. The 500-MHz processor is available in a 23×23-mm^2, 288 contact-ball BGA package. The 600-MHz, standard-temperature processor is also in volume production. Both processors cost $49.50 (10,000).

Texas Instruments, www.ti.com

Digital power-supply controller targets switch-mode power supplies

Providing digital power-control and -management functions for most isolated and nonisolated switch-mode-power-supply topologies, the Si825x single-chip family of digital power-supply controllers incorporates hardware for real-time loop control and a flash-based system-management controller. The control loop updates at a 10-MHz rate and features a dedicated ADC, a programmable DSP-filter engine, a six-channel PWM, and a programmable overcurrent-protection hardware detector. Based on a 50-MIPS 8051 CPU with 32 kbytes of flash memory, the controller includes a 12-bit self-sequencing ADC, an SMBus/PMBus-interface port, a UART, 16-bit timers, and additional PWM channels. The controller performs fault detection and recovery; control-loop optimization, including dynamic-loop compensation and dead-time adjustment; PMBus communication; and external-device management. The Si825x comes in a 5×5-mm QFN-28 or

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LQFP-32 package with an operating-temperature range of −10 to +125°C and sells for $2.49 (1000).
Silicon Laboratories Inc, www.silabs.com

CCID class driver provides USB support for smart-card applications

A new class driver for the Nucleus USB software offers USB support for the Nucleus RTOS. The Nucleus CCID class driver connects the embedded host and smart-card reader without an additional driver. The vendor released the driver for use with the Nucleus host stack software. The software complies with USB 1.1 and USB 2.0. The software is licensed with source codes and starts at $14,995, and the license for the class drivers is $2995.
Accelerated Technology, www.acceleratedtechnology.com

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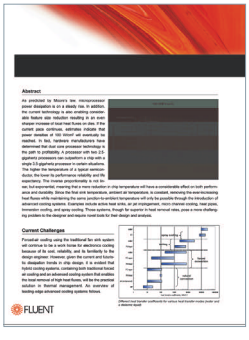
METHODS FOR EVALUATING ADVANCED ELECTRONICS COOLING SYSTEMS



This white paper presents the pros and cons for several advanced electronics cooling systems. Such complex systems require novel tools for their design and analysis. The benefits of one proven technology tool are discussed. Download your complimentary white paper: http://www.fluent.com/direct/edn
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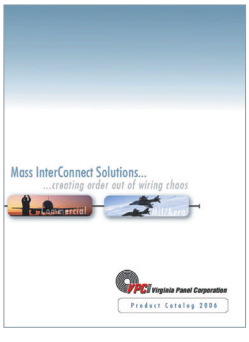

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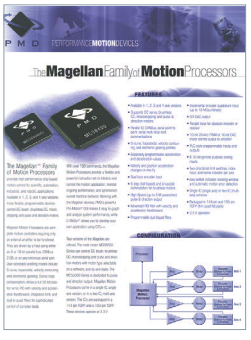

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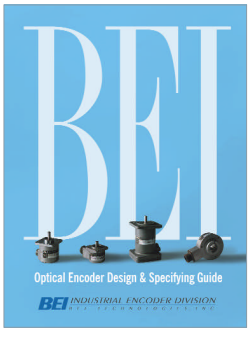

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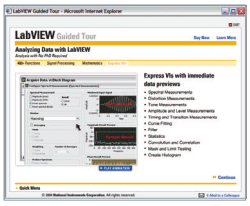

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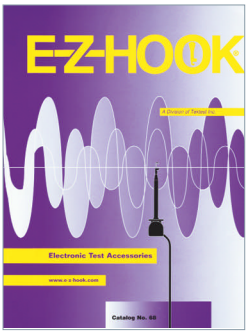

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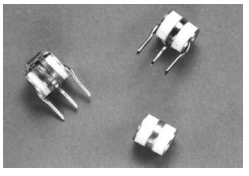

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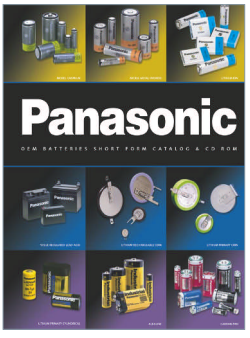

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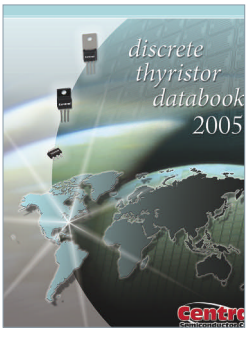

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STATS SiGe should grow 40% to $1.6 billion / GaAs should grow 10% to $3.5 billion

SiGe gets GaAs

GaAs (gallium arsenide) was the ultimate semiconductor technology for the ultra-high-speed logic elements in supercomputers before silicon reached the gigahertz range. About 20 years ago, designers adapted this niche process technology to analog circuits for mass-market applications in which both power levels and bandwidth are pushing the edge. Today, GaAs is the leading technology in cellular power amplifiers.

However, the days of GaAs in many of these applications may be numbered. Nearly as fast, though less power-capable, SiGe (silicon germanium) uses a cheaper process that is largely compatible with the ubiquitous silicon-design and fab technologies (see "SiGe gets real," *EDN*, June 24, 1999). According to Robert Castellano, PhD, of research source The Information Network (www.theinformationnet.com), whereas SiGe sales are currently just half those of GaAs, SiGe has much higher annual growth. Although GaAs is a better fit for the multiwatt demands of some wireless applications, SiGe is a good match for the less-than-1W needs of WiFi (Wireless Fidelity) and other low-power systems. Further, SiGe lets designers embed logic and power-management functions onto the die.—by Bill Schweber, Executive Editor

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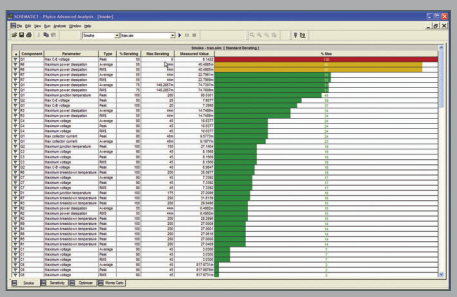

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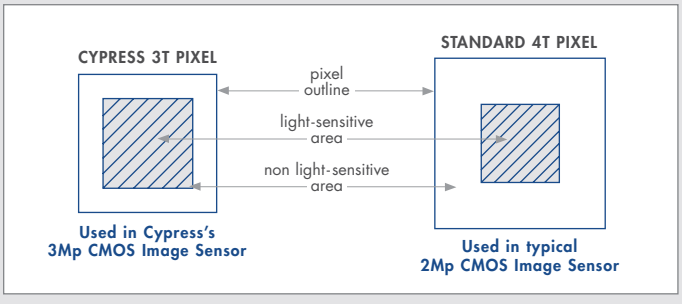

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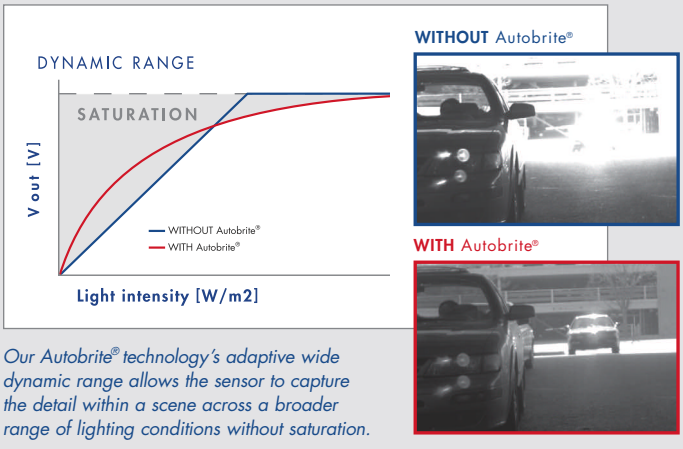

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